ROLL NO. _____

Code: AC58/AT58/AC106/AT106 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT (Current & New Scheme)

Time: 3 Hours **December - 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. When the CPU detects an interrupt, it than saves its
(A) current state **(B)** next state
(C) previous state **(D)** Both **(A)** & **(B)**

b. The registers, the ALU, and the interconnecting bus are collectively referred to as the _____.
(A) Datapath **(B)** Subpath
(C) Connecting path **(D)** None of these

c. Von Neumann architecture is
(A) SIMD **(B)** SISD
(C) MIMD **(D)** MISD

d. In immediate addressing the operand is placed
(A) in the CPU register **(B)** in stack
(C) in memory **(D)** after OP code in the instruction

e. MFC stands for
(A) Memory Format Caches **(B)** Memory Find Command
(C) Memory Function Complete **(D)** Mass Format Command

f. A 16-bit computer that generates 16-bit addresses is capable of addressing upto _____ memory locations.
(A) 64K **(B)** 16K
(C) 1028K **(D)** 16M

g. A k-bit field can specify any one of
(A) 3k registers **(B)** K3 registers
(C) K2 registers **(D)** 2k registers

h. Pipelining strategy is called, implement
(A) instruction execution **(B)** instruction prefetch
(C) instruction decoding **(D)** instruction manipulation

i. Memories that consist of circuits capable of retaining their state as long as power is applied are known as _____.
(A) static memory **(B)** power memory
(C) dynamic memory **(D)** circuit memory

j. Interrupts which are initiated by an Instruction are
(A) internal **(B)** external
(C) hardware **(D)** software

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Name & briefly describe the different generations of computer system. **(8)**

b. Consider the following instruction:
C ← [A] + [B]
Explain the two-phase execution procedure of the statement? **(8)**

Q.3 a. Explain with examples the difference between arithmetic shift and logical shift. **(8)**

b. A two word instruction is stored in memory at an address designated by symbol *W*. The address field of the instruction (stored at *W* + 1) is designated by the symbol *Y*. The operand used during the execution of the instruction is stored at an address symbolized by *Z*. An index register contains the value *X*. State how *Z* is calculated from the other addresses if the addressing mode of the instruction is:
(i) Direct (ii) Indirect
(iii) Relative (iv) Indexed **(8)**

Q.4 a. List out the sequence of operations involved in handling an interrupt request from a single device. **(8)**

b. What do you mean by Bus Arbitration? Discuss two approaches to bus arbitration: Centralized and Distributed. **(8)**

Q.5 a. What are the needs for input-output interface? Explain the functions of a typical 8-bit parallel interface in detail. **(8)**

b. With a block diagram, explain how a keyboard is connected to a processor? **(8)**

Q.6 a. Consider a memory consisting of 64K words of 8 bits each. Give the organization to implement this memory using 16K X 1 static memory chips. **(8)**

b. Explain the following mapping procedure:
(i) Direct mapping (ii) Associative mapping **(4+4)**

Q.7 a. Design a half adder as a 2 level AND OR circuit. Implement full adder circuit using 2 half adder. **(8)**

b. Explain with the help of a diagram, virtual memory organization. **(8)**

Q.8 a. Explain two techniques for speeding up the multiplication operation. **(8)**

b. Explain the floating point Addition – subtraction unit with neat diagram. **(8)**

Q.9 a. Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction. **(8)**

b. With the help of figure, explain multiple-bus organization. **(8)**