ROLL NO. _____

Code: AC103/AT103 Subject: ANALOG & DIGITAL ELECTRONICS

AMIETE – CS/IT *{NEW SCHEME}*

Time: 3 Hours **December - 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Typical value of forward voltage drop for silicon diode is
(A) 0.3 V **(B)** 0.4 V
(C) 0.5 V **(D)** 0.7 V

b. A diode that finds its application as voltage reference source is known as
(A) Light Emitting diode **(B)** Photo diode
(C) Zener diode **(D)** Varactor diode

c. With the same secondary voltage and filter, which has the most ripples?
(A) Half-wave rectifier **(B)** full-wave rectifier
(C) Bride rectifier **(D)** Impossible to say

d. The base of an NPN transistor is thin and
(A) heavily doped **(B)** metallic
(C) lightly doped **(D)** doped by a pentavalent material

e. The current gain of a BJT is the ratio of the
(A) collector current to emitter current
(B) collector current to base current
(C) emitter current to collector current
(D) base current to collector current

f. Attach an even-parity bit to the BCD code for decimal 69
(A) 101101001 **(B)** 011101001
(C) 111101001 **(D)** 001101001

g. What is the minimum number of 2-input NOR gates required to realize a 2-input exclusive NOR (XNOR) gate?
(A) 3 **(B)** 4
(C) 5 **(D)** 6

h. What is the minimum number of 2-input NAND gates required to realize a half adder circuit.
(A) 4 **(B)** 5
(C) 6 **(D)** 3

i. How many flip flops are required to convert a mod-8 counter into mod-64 counter?
(A) 1 **(B)** 2
(C) 3 **(D)** 4

j. What is the output frequency of decade counter that is clocked from a 50 kHz clock signal
(A) 20 kHz **(B)** 10 kHz
(C) 4 kHz **(D)** 5 kHz

PART A
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Explain the impact of junction temperature on reverse saturation current of a semiconductor pn-junction. **(8)**

b. Determine the levels of reverse saturation current (*Is*) at temperatures of 35℃ and 45℃ for a junction which has reverse saturation current (*Is*) = 30 nA at 25℃. **(8)**

Q.3 a. Draw circuit diagram of full-wave rectifier for producing a positive output voltage. Sketch the input and output wave forms and explain the circuit operation. **(8)**

b. Draw circuit diagram of full-wave voltage doubler. Sketch suitable diagram to explain the circuit operation. **(8)**

Q.4 a. Establish relationship among various currents in a PNP BJT when its base-emitter junction is forward biased and base-collector junction is reverse biased. **(8)**

b. Calculate collector current (I_C) and emitter current (I_E) for a BJT that has α_{dc} = 0.98 and I_B = 100 μA. Determine the value of β_{dc} for the BJT. **(8)**

Q.5 a. Draw circuit diagram of an NPN BJT based single-stage common-emitter (CE) amplifier with resistive voltage divider biasing scheme. **(8)**

b. Draw circuit diagram of an NPN BJT based phase shift oscillator with RC phase shift network. **(8)**

PART B
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Describe parallel and serial transmission of digital data and relative advantage of parallel and serial transmissions. **(8)**

b. Convert the following
(i) $(82.25)_{10}$ = ( )$_{16}$
(ii) $(374.26)_8$ = ( )$_2$
(iii) $(1110100.0100111)_2$ = ( )$_8$
(iv) $(17E.F6)_{16}$ = ( )$_2$ **(8)**

Q.7 a. Briefly describe De Morgan's theorem and duality theorem. **(8)**

b. Design a 2-input exclusive OR (XOR) gate only with minimum number of 2-input NAND gates. **(8)**

Q.8 a. Design a 4-bit adder/subtractor circuit that performs addition/subtraction with the help of a control signal M using 2's complement method for subtraction. **(8)**

b. Explain the operation of the 4-bit adder/subtractor circuit that performs addition/subtraction with the help of a control signal using 2's complement method for subtraction. **(8)**

Q.9 a. Draw gate-level schematic of JK flip-flop realized only with 2-inut NAND gates and having PRESET and CLEAR control signals. **(8)**

b. Explain the operation of JK flip-flop realized only with 2-inut NAND gates and having PRESET and CLEAR control signals. **(8)**