ROLL NO. _____

Code: DE58 / DC58 **Subject: LOGIC DESIGN**

DipIETE – ET/CS

Time: 3 Hours **DECEMBER 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. A digital system that uses n-bits can go through_____

(A) n^2-1 **(B)** 2^n
(C) 2^n-1 **(D)** 2^{n-1}

b. The 2's complement of the decimal -4 is _____

(A) 0100 **(B)** 1100
(C) 1010 **(D)** 1011

c. Gray code is _____

(A) Non weighted code **(B)** Cyclic code
(C) Reflected code **(D)** All of these

d. ROM contains _____

(A) Programmable AND array and programmable OR array
(B) Programmable AND array and non-programmable OR array
(C) Non-programmable AND array and programmable OR array
(D) Non-programmable AND array and non-programmable OR array

e. Using N flip-flops would produce an output frequency from the last flip-flop equal to _____ of the input frequency.

(A) same **(B)** one fourth
(C) half **(D)** three fourth

f. The number of flip-flops required for MOD-16 ring counter are _____

(A) 2 **(B)** 4
(C) 16 **(D)** 32

g. A four bit binary adder could be constructed with a minimum of

(A) 3 one-bit full adder and a half adder
(B) 4 one-bit full adder
(C) 4 half adders
(D) None of these

h. A five bit Johnson counter in cascade with a five bit ring counter produces a frequency divider of _____

(A) 25 **(B)** 10
(C) 50 **(D)** 15

i. The decoding glitches are far more likely to occur in the case of _____

(A) Ripple counter **(B)** Parallel counters
(C) Johnson counter **(D)** Ring counter

j. Multiplexers are used in

(A) Data Selection **(B)** Logic function generation
(C) Parallel to Serial conversion **(D)** All of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. In a base-5 number system, 3 digit representations is used. Find out (i) Number of distinct quantities that can be represented.(ii) Representation of highest decimal number in base-5. **(4)**

b. In a signed representation given binary string is $(11101)_2$. What will be the sign and magnitude of the number represented by this string in signed magnitude, 1's complement and 2's complement representation? **(6)**

c. Convert the hexadecimal 2AC5.D to decimal, octal and binary. **(6)**

Q.3 a. Obtain (a) minimal sum of product (b) minimal product of sum expression for the function F(w, x y, z) = Σ (0, 2, 3, 6, 7, 8, 10, 11, 12, 15). **(6)**

b. Implement a three-input EX-NOR function using only two-input EX-NOR gates. **(5)**

c. A'B+C'D is a simplified Boolean expression of the expression A'B'C'D+A'B'C'D+A'B. Determine if there are any 'don't care' entries. **(5)**

Q.4 a. The 100 kHz square waveform of **Fig. 1(a)** is applied to the clock input of the flip-flops shown in **Figs. 1(b)** and **(c)**. If the Q output is initially '0', draw the Q output waveform in the two cases. Also, determine the frequency of the Q output in the two cases. **(8)**

Fig.1(a)

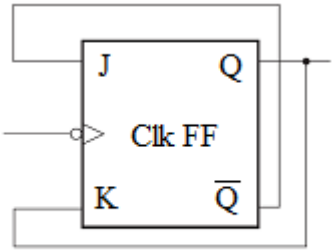

Fig.1(b)

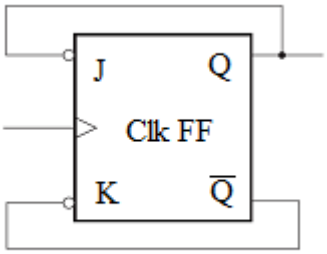

Fig.1(c)

b. Design a mod-3 counter using JK flip-flop and explain its operation with the help of waveform. **(8)**

Q.5 a. Design a 4 bit serial adder with the help of neat diagram. **(8)**

b. Determine the number of half and full adder circuit blocks required to construct a 64-bit binary parallel adder. Also, determine the number and type of additional logic gates needed to transform this 64-bit adder into a 64-bit adder–subtractor. **(8)**

Q.6 a. Distinguish between asynchronous and synchronous flip-flops. Design a 4 bit universal synchronous counter using JK flip-flops. **(6)**

b. Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010, _ _ _ Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. Use J-K flip-flops. What will the counter hardware look like if the unused states are to be considered as 'don't care's. **(6)**

c. Determine the modulus of the presettable counter shown in **Fig. 2**. If the counter were initially in the 0110 state, what would be the state of the counter immediately after the eighth clock pulse be? **(4)**

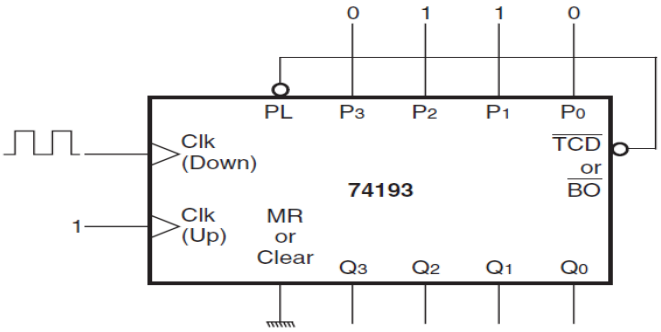

Fig.2

Q.7 a. Use an 8 input MUX to implement the following equation:
Y = A'.B'.C'.D' + A'.B'.C.D + A'.B.C'.D + A'.B.C'.D' + A.B'.C'.D + A.B'.C.D'+ A.B.C'.D' + A.B.C'.D. **(8)**

b. Implement the functions defined by the following truth table in **Fig.3** using a decoder and NAND gates. **(4)**

A	B	C	Y_1	Y_2
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

Fig.3

c. What is priority encoder? Design a 4x2 priority encoder. **(4)**

Q.8 a. Draw the diagram of four bit universal shift register and explain its operation. **(8)**

b. Refer to the logic circuit of **Fig.3**. Determine the modulus of this counter and write its counting sequence. **(8)**

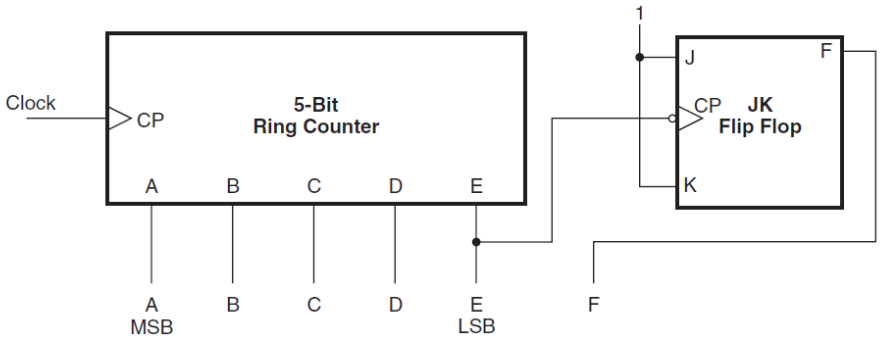

Fig.4

Q.9 a. It is required to obtain an 8K × 8 memory system for 8085 microprocessor system that has an addressing capability of 64K locations. Given memories are 2K × 8 ROM ICs and 2K × 8 RAM ICs. Obtain the exhaustive decoded system, which maps the 8K-memory system to begin from 8000H. **(8)**

b. Draw the general structure of DRAM and explain it. Also compare it with SRAM. **(8)**