ROLL NO. _____

Code: DE56 **Subject: ANALOG ELECTRONICS**

DipIETE – ET

Time: 3 Hours **DECEMBER 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The most popular form of IC package is

(A) TO-5 **(B)** DIL
(C) Flat Pack **(D)** All of these

b. The CC amplifier configuration has:

(A) high input impedance and high output impedance
(B) high input impedance and low output impedance
(C) low input impedance and high output impedance
(D) low input impedance and low output impedance

c. MOSFET uses the electric field of

(A) gate capacitance to control the channel current
(B) barrier potential of p-n junction to control the channel current
(C) both **(A)** and **(B)**
(D) none of these

d. The practical maximum efficiency for a class A power amplifier is usually:

(A) 25% **(B)** 50%
(C) 75% **(D)** none of these

e. The voltage gain of an OPAMP voltage follower is:

(A) zero **(B)** unity
(C) infinite **(D)** very high

f. The voltage gain of an inverting amplifier using OPAMP is

(A) $-\frac{R_f}{R_i}$ **(B)** $\frac{R_f}{R_i}$

(C) $1+\frac{R_f}{R_i}$ **(D)** $1-\frac{R_f}{R_i}$

g. All MOS OPAMPs are:

(A) more compact **(B)** consume high power
(C) low CMMR value **(D)** none of these

h. In an amplifier that employs a P-Channel JFET, the device can usually be replaced with an N-channel JFET having similar specifications, provided that:

(A) All the resistors are reversed in polarity for the circuit in question
(B) The power supply polarity is reversed for circuit in question
(C) The drain, rather than the source, is placed at signal ground
(D) The output is taken from the source, rather than the drain

i. What does the discharge transistor do in the IC 555 timer circuit?

(A) Charges the external capacitor to stop the timing
(B) Charges the external capacitor to start the timing over again
(C) Discharges the external capacitor to stop the timing
(D) Discharges the external capacitor to start the timing over again

j. An astable multivibrator has:

(A) one stable state
(B) both stable states
(C) one stable state and one quasi-stable state
(D) both quasi-stable states

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is epitaxial layer? Describe one way which it can be created. **(3+3)**

b. Describe the methods used to fabricate capacitors in monolithic integrated circuits. **(6)**

c. It is desired to fabricate a 1.5 kΩ resistors using a diffused P Layer having sheet resistance 200Ω/squares. **(4)**
(i) What aspect ratio should the resistor have?
(ii) What should be the total length of the diffused region?

Q.3 a. In an NPN silicon transistor $\alpha = 0.995$, $I_E = 10mA$, leakage current $I_{CBO} = 0.5\mu A$. Determine I_C, I_B, β, I_{CEO} **(6)**

b. Draw an h-parameter equivalent circuit for the CE circuit with voltage divider bias, a bypassed emitter resistor, a capacitor coupled signal source and capacitor coupled load. Briefly explain. **(10)**

Q.4 a. Explain the operating Principle of N channel JFET. **(4)**

b. Explain how an FET can be used as an Amplifier? **(4)**

c. An N channel JFET has a pinch-off voltage of –4.5 V and I_{DSS} = 9mA **(8)**

(i) At what value of V_{GS} in the pinch-off region will I_D = 3mA
(ii) What is the value of $V_{DS(sat)}$ when I_D = 3mA

Q.5 a. Explain how LED different from an ordinary pn junction diode? Describe its construction in brief. **(4+4)**

b. Two amplifier stages are required to be coupled by a coupling transformer, if the output impedance of first stage is 12 kΩ while the input impedance of the second stage is 3 kΩ. What should be the inductance of primary and secondary of the transformer so that prefect matching be obtained at a frequency of 250 Hz. **(8)**

Q.6 a. What are the characteristics of ideal OPAMP? **(4)**

b. Define the following parameters: **(4)**
(i) Input bias current
(ii) CMMR
(iii) Slew Rate
(iv) Input offset voltage

c. When the inputs to a certain differential amplifier are $v_{i1} = 0.1 \sin\varphi t$ and $v_{i2} = -0.1 \sin\varphi t$. It is found that outputs are $v_{O1} = -5 \sin\varphi t$ and $v_{O2} = 5 \sin\varphi t$. When both inputs are $2 \sin\varphi t$, the outputs are $v_{O1} = -0.05 \sin\varphi t$ and $v_{O2} = 0.05 \sin\varphi t$. Find the CMMR in dB. **(8)**

Q.7 a. Draw and explain the working of OPAMP integrator. Draw input and output waveforms of the circuit. **(5+3)**

b. Design a practical differentiator that will differentiate signals with frequencies upto 200 Hz. The gain at 10 Hz should be 0.1 **(8)**

Q.8 a. What are the applications of Schmit Trigger? Explain the operation of Schmit Trigger. **(8)**

b. Draw the circuit of a Monostable Multivibrator using IC 555 timer and explain its operation. **(8)**

Q.9 a. Explain the basic technique used for DAC. **(4)**

b. List the features of LM 723 Voltage Regulator. **(6)**

c. As shown in **Fig.1** Vin = 20V, R = 200Ω and Vz = 12V. If V_{BE} = 0.65V, **(6)**

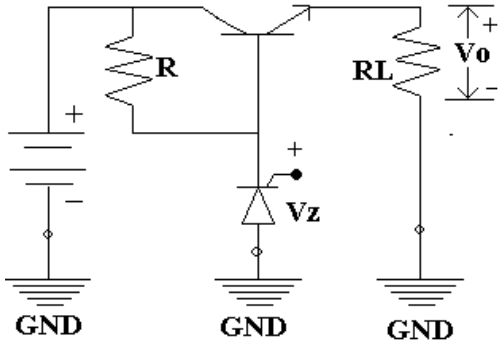

Fig.1

find
(i) Vo
(ii) The collector to emitter voltage of the pass transistor and
(iii) The current in the 200Ω resistor