ROLL NO. _____

Code: AE74 **Subject: VLSI DESIGN**

AMIETE – ET

Time: 3 Hours **DECEMBER 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The unit of power density is

(A) W/cm^3 **(B)** cm^3
(C) W/cm^2 **(D)** W^3

b. A layer of SiO_2 is grown all over the surface of the wafer to

(A) Achieve an even distribution **(B)** Protect UV light
(C) Protect Surface **(D)** All of these

c. The MOS transistor conductance is given by

(A) $g_m = \beta(Vgs - Vt)$ **(B)** $g_m = \beta / (Vgs - Vt)$
(C) $g_m = (Vgs - Vt) / \beta$ **(D)** $g_m = \beta(Vgs - Vt)\ V_{SB}$

d. The minimum transit time for an electron to travel from source to drain can be calculated as

(A) $V_{drift}=\mu/E$ **(B)** $V_{drift} = E/\mu$
(C) $V_{drift}=\mu E$ **(D)** $V_{drift}=\mu E/d$

e. Metal can cross poly-silicon or diffusion without any significant effect

(A) TRUE **(B)** FALSE
(C) VIA is required **(D)** Interconnection Forms

f. In Lambda based rules, λ is related to

(A) Interconnect Length **(B)** Oxide Layer
(C) Poly Layer **(D)** Resolution of the process

g. The total propagation delay time T in Carry Skip Adder is given by

(A) $T = n/M$ **(B)** $T = 2 (P–1) K_1 + (M–2) K_2$
(C) $T = 2 (P–1) K_1$ **(D)** $T = M/n$

h. The dynamic power consumption P_d can be written as

(A) $P_d = C_L V_{DD} f$ **(B)** $P_d = C_L V^2_{DD} f$
(C) $P_d = m (C_L V^2_{DD} f)$ **(D)** None of these

i. The gate area of the device is

(A) $A_g = C_{ox} L W$ **(B)** $A_g = L W$

(C) $A_g = LW/C_{ox}$ **(D)** $A_g = C_o L$

j. The Volatile memories are

(A) DRAM **(B)** SRAM
(C) ROM **(D)** EPROM

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Compare the available technologies in IC's Design. **(4)**

b. With neat sketch explain the enhancement mode transistor action. **(8)**

c. Draw the cross sectional view of CMOS –inverter (P-WELL). **(4)**

Q.3 a. Explain CMOS inverter with all the region of operations. **(8)**

b. Define Stick Diagram. Explain the CMOS encodings in it. **(8)**

Q.4 a. Write the circuit and stick diagram for: **(8)**
(i) two input CMOS NOR gate
(ii) f = [(xy) + z]'

b. Draw and explain nMOS enhancement mode pull-up and transfer characteristic. **(8)**

Q.5 a. Write short notes on – (i) Contact and Via Resistance (ii) Silicides **(8)**

b. Draw the schematic of Inverting Type nMOS Super Buffer and explain its functionality briefly. **(8)**

Q.6 a. Discuss the Limitations of Scaling in VLSI Designs. **(8)**

b. Explain Structured Design Approach – Regularity with example. **(8)**

Q.7 a. Design and explain 4 X 4 barrel shifter. **(8)**

b. Explain how to implement ALU functions with an adder? **(8)**

Q.8 a. Write the circuit of one transistor dynamic RAM cell and explain briefly read and write functions. **(8)**

b. Explain the optimization of CMOS Inverters. **(8)**

Q.9 a. Explain the different requirements of large system designs in silicon. **(8)**

b. Explain how the interface with the fabrication house designer must establish. **(8)**