ROLL NO. _____

Code: AE68 **Subject: EMBEDDED SYSTEMS DESIGN**

AMIETE – ET

Time: 3 Hours **DECEMBER 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. An embedded system must have

(A) Hard disk
(B) Processor and memory
(C) Operating system
(D) Processor and input-output unit(s)

b. The circuitry for transforming data and for storing temporary data is known as

(A) Datapath
(B) Datastore
(C) Device-track
(D) Datalink

c. Sophisticated embedded systems development requires

(A) IPs and several ASIPs
(B) IPs and several ASIPs, and hardware- software co-design
(C) Multi-core processors
(D) System on-chip with large memory

d. Identify the true statement from the following:
RTOS is used in most embedded systems when the system does

(A) Concurrent processing of multiple real time processes
(B) Sequential processing of multiple processes when the tasks have real time constraints
(C) Real time processing of multiple processes
(D) The concurrent processing of multiple processes, tasks have real time constraints and deadlines, and high priority task preempts low priority task as per the real time constraints.

e. Hard real time operating system has _____ jitter than a soft real time operating system.

(A) Less
(B) More
(C) Equal
(D) None of these

f. For real time operating systems, interrupt latency should be

(A) Minimal **(B)** Maximum
(C) Zero **(D)** Dependent on the scheduling

g. ROM is type of _____

(A) Semiconductor **(B)** Firmware
(C) Adaptor **(D)** Volatile memory

h. In immediate addressing, the operand field contains

(A) Data itself
(B) Address location of the data
(C) Address location of the base register
(D) Pointer to the address location of the data

i. Time duration required for scheduling dispatcher to stop one process and start another is known as

(A) Process latency **(B)** Dispatch latency
(C) Execution latency **(D)** Interrupt latency

j. The code that changes the value of the semaphore is _____.

(A) Remainder section code **(B)** Essential section code
(C) Critical section code **(D)** None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Mention the characteristics of embedded systems. **(6)**

b. Illustrate with a diagram the working of a single-purpose processor. **(5)**

c. Discuss the optimizing design metrics in the design of embedded systems. **(5)**

Q.3 a. Write a program in assembly language to clear an array M[256]. Assuming M starts at location 256 (and thus ends at location 511).Write the assumptions for the assembly language code. **(6)**

b. What are the different stages of execution of instructions? **(4)**

c. Write the benefits of choosing a single purpose processor over a general purpose processor. **(6)**

Q.4 a. A particular motor operates at 10 revolutions per second when its controlling input voltage is 3.7 V. Assume that you are using a microcontroller with a PWM whose output port can be set high (5 V) or low (0 V). (i) Compute the duty cycle necessary to obtain 10 revolutions per second. (ii) Provide values for a pulse width and period that achieve this duty cycle. **(8)**

b. Describe the working of an UART. **(8)**

Q.5 a. Write any two cache replacement policies. **(4)**

b. From the given following three cache designs, find the one with the best performance by calculating the average cost of access. Show all calculations.

(i) 4 Kbyte, 8-way set-associative cache with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles
(ii) 8 Kbyte, 4-way set-associative cache with a 4% miss rate; cache hit costs two cycles, cache miss costs 12 cycles.
(iii) 16 Kbyte, 2-way set-associative cache with a 2% miss rate; cache hit costs three cycles, cache miss costs 12 cycles. **(9)**

c. What is DRAM? **(3)**

Q.6 a. Illustrate the functioning of two protocol control methods: **(6)**
(i) Strobe
(ii) Handshake

b. Discuss the steps of Arbitration using a priority arbiter. **(4)**

c. What are Interrupts? What is an ISR? How is it invoked? **(6)**

Q.7 a. Give an example to use Semaphore as a signalling device. **(7)**

b. What are the problems of shared data and how are they removed? **(5)**

c. Explain the function of a scheduler. **(4)**

Q.8 a. What is a pipe? **(2)**

b. Discuss the rules to be followed by Interrupt Routines in an RTOS environment. **(6)**

c. Write a pseudocode to delay a task by using RTOS delay Function. **(8)**

Q.9 a. What is hard real time scheduling? **(2)**

b. What do you mean by encapsulating semaphore? Write a program to show how a semaphore is encapsulated. **(8)**

c. Discuss briefly about the ways by which memory space can be conserved. **(6)**