ROLL NO. _

Code: AE66/AC66/AT66 Subject: MICROPROCESSORS & MICROCONTROLLERS

AMIETE - ET/CS/IT

DECEMBER 2014 Time: 3 Hours Max. Marks: 100 PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER. NOTE: There are 9 Ouestions in all. • Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else. The answer sheet for the 0.1 will be collected by the invigilator after 45 minutes of the commencement of the examination. Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks. • Any required data not explicitly given, may be suitably assumed and stated. **Q.1** Choose the correct or the best alternative in the following: (2×10) a. Sign magnitude notation of +7 and -5 is (A) 0111 and 1101 **(B)** 1111 and 1101 (C) 0101 and 1111 **(D)** 0101 and 0111 b. LS byte portion of 16 bit address is received in register. (A) W **(B)** A (**C**) Z (D) None of these c. Which interrupt has the second highest priority among the following. (A) TRAP (B) RST 7.5 (C) RST 5.5 (D) INTR d. What should be the input to common anode type seven segment display interface to display character 3. (A) ODH **(B)** BDH (C) OOH (D) DOH e. 8 bit slave register is used in (A) 8255 **(B)** 8085 (C) 8259 (D) None of these f. In asynchronous transmission mode the transmission of characters is done at (A) Regular intervals **(B)** Irregular intervals (C) Synchronised with the clock (**D**) None of these

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g. To which mode 8253 should be configured to make it work as a square wave generator

(A) mode 1	(B) mode 2
(C) mode 3	(D) mode 0

h. In 8085 name the 16 bit registers

(A) SP	(B) PC
(C) IR	(D) Both (A) & (B)

i. 8085, is reset by placing a logic 0 on RESET-IN pin for atleast ______after power is supplied to Vcc pin

(A) 0.5 μs	(B) 0.5 ms
(C) 0.5 s	(D) 0.5 ns

j. Which addressing mode is not supported by 8051 microcontroller.

(A) Register Addressing	(B) Implied Addressing
(C) Indexed Addressing	(D) Absolute Addressing

Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

Q.2	a.	Explain with example the following set of instructions: (i) MVI M, d8 (ii) LDAX r_p (iii) XCHG (iv) STAX r_p	(4)
	b.	Explain different flag registers present in 8085.	(4)
	c.	Discuss different stack operation instructions of 8085. (any four)	(8)
Q.3	a.	Differentiate between CALL and JUMP instruction of 8085 and ment various conditional call instructions.	tion (8)
	b.	Explain the instruction cycle steps in 8085 microprocessor.	(8)
Q.4	a.	Write an 8085 assembly language program to exchange 10 bytes of data sto from location x with 10 bytes of data stored from location y.	red (8)
	b.	Write 8085 assembly language program along with flow chart to find smallest of N 1-byte numbers. The N value is provided at location X, and no's are present from location $X+1$. Display the smallest no in data field its location in address field.	the the and (8)
Q.5	a.	Explain in detail status check data transfer scheme with the help of a fl chart.	low (8)

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Code: AE6	66/A	C66/AT66 Subject: MICROPROCESSORS & MICR	OCONTROLLERS
	b.	With necessary waveforms, explain the need for INTR and INTA action taken by 8085 when INTR pin is activated.	A* pins and (8)
Q.6	a.	Discuss the following w.r.t. 7 segment display interface: (i) Layout of 7 segment display (ii) Internal circuitry of 7 segment common anode display (iii) Condition for glowing of a LED.	(6)
	b.	Give the description of matrix keyboard interface.	(6)
	c.	Explain the following pins w.r.t. INTEL 8279 (i) C / D (ii) RD* (iii) Shift (iv) B_{3-0}	(4)
Q.7	a.	Explain all the registers used in 8259.	(8)
	b.	What is DMA? Explain the need for DMA data transfer.	(4)
	c.	Mention the conditions for the following modes w.r.t. 8257 (i) When processor is the master & 8257 is slave. (ii) When processor is in HOLD state & 8257 is in master mode.	(4)
Q.8	a.	Explain the status port of 8251.	(8)
	b.	Explain the internal architecture of 8253.	(8)
Q.9	a.	Write the simplified block diagram of 8051 microcontroller.	(8)
	b.	Explain internal RAM organization of 8051.	(8)

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