ROLL NO. _____

Code: AE54/AC54/AT54 Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT

Time: 3 Hours **DECEMBER 2014** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):

(A) Ex-NOR gate **(B)** OR Gate
(C) Ex-OR Gate **(D)** NAND Gate

b. Determine the values of A, B, C, and D that make the sum term $\bar{A}+B+\bar{C}+D$ equal to zero.

(A) A = 1, B = 0, C = 0, D = 0 **(B)** A = 1, B = 0, C = 1, D = 0
(C) A = 0, B = 1, C = 0, D = 0 **(D)** A = 1, B = 0, C =1, D =1

c. The output of an exclusive-NOR gate is 1. Which input combination is correct?

(A) A = 1, B = 0 **(B)** A = 0, B = 1
(C) A = 0, B = 0 **(D)** none of these

d. How is a J-K flip-flop made to toggle?

(A) J = 0, K = 0 **(B)** J = 1, K = 0
(C) J = 0, K = 1 **(D)** J =1, K = 1

e. A MOD-16 ripple counter is holding the count 1001_2. What will the count be after 31 clock pulses?

(A) 1000_2 **(B)** 1010_2
(C) 1011_2 **(D)** 1101_2

f. Refer to Fig. 1, if the value of R_1 decreases, the voltage gain will _____ and the input impedance will _____.

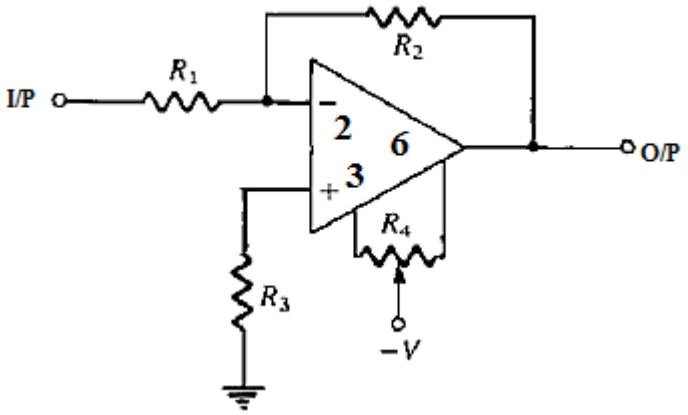

Fig.1

(A) increase, increase respectively **(B)** increase, decrease respectively
(C) decrease, decrease respectively **(D)** decrease, increase respectively

g. What is the slew rate of an op-amp if the output voltages change from 2 V to 3 V in 0.2 ms?

(A) 5 V/ms **(B)** 3 V/ms
(C) 2 V/ms **(D)** 1 V/ms

h. The _____ is defined as the time the output is active divided by the total period of the output signal.

(A) on time **(B)** off time
(C) duty cycle **(D)** active ratio

i. Which mode of operation is being used when a 555 timer chip has two external resistors and an external capacitor?

(A) monostable **(B)** pulse stretching
(C) Schmitt triggering **(D)** astable

j. The resolution of a 0–5 V, 6-bit digital-to-analog converter (DAC) is

(A) 63% **(B)** 64%
(C) 1.56% **(D)** 15.6%

PART (A)
Answer At least TWO questions. Each question carries 16 marks.

Q.2 a. Give the classification of different IC technologies. **(4)**

b. For a differential amplifier using ideal op-amp(Shown in Fig. 2)

(i) Find the output voltage v_o

(ii) Show that the output corresponding to common-mode voltage $v_{CM} = \frac{(v_1 - v_2)}{2}$ is zero if $\frac{R'}{R} = \frac{R_2}{R_1}$

(iii) Find CMRR of the amplifier if $\frac{R'}{R} \neq \frac{R_2}{R_1}$ **(12)**

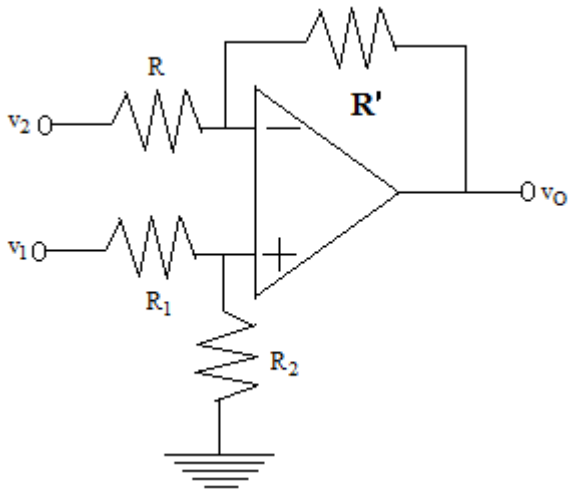

Fig.2

Q.3 a. Draw and explain the circuit diagram of the voltage to current converter (Transconductance Amplifier). **(8)**

b. Explain the following non-ideal dc characteristics of real op-amp:
(i) Input bias current
(ii) Input offset current
(iii) Input offset voltage
(iv) Thermal drift **(8)**

Q.4 a. Design a circuit diagram of non-inverting integrator, also derive it's input output relation. **(8)**

b. Design a circuit diagram of zero crossing detector using op-amp as comparator. **(8)**

Q.5 a. Describe the pin diagram of 555 timer IC and give examples of its application. **(4)**

b. Design a circuit diagram of 3 bit R-2R Ladder DAC and also derive it's input output relation. **(6)**

c. Explain the working of Series Op-Amp voltage regulator with its circuit diagram. **(6)**

PART (B)
Answer At least TWO questions. Each question carries 16 marks.

Q.6 a. What are alphanumeric codes? Give suitable example and numbers of bits in the code? **(3)**

b. What is the advantage and disadvantage of encoding a decimal number in BCD as compared with straight binary? **(3)**

c. Perform the following conversions:
(i) $(1011.0011)_2 = (\_\_\_\_)_{10}$ (ii) $(204.125)_{10} = (\_\_\_\_)_{16}$
(iii) $(25.25)_{10} = (\_\_\_\_)_2$ (iv) $(B4.C9)_{16} = (\_\_\_\_\_)_{10}$
(v) $(5431.4)_8 = (\_\_\_\_)_{16}$ **(5×2)**

Q.7 a. What are the advantages of digital systems over analog systems? **(4)**

b. Minimize the given expression by using Boolean algebra,
$Y = B(1+C)(B+\overline{B}C)(B+D)$ **(4)**

c. Design a combinational logic circuit with three input variables(say A, B, C) that produce a logic 1 output (say Y)when more than one input variables are logic 1.Draw the truth table and minimize expression using k-map. **(8)**

Q.8 a. What is Multiplexer? Draw the logic diagram and functional table for the 4×1 MUX. **(8)**

b. Design a Full Adder Circuit using two Half adder circuits and other basic gate? **(8)**

Q.9 a. Compare between Synchronous sequential circuits and asynchronous sequential circuits? **(4)**

b. Draw the circuit diagram of J-K flip-flop using NAND gate and draw the truth table and excitation table of J-K flip-flop. **(6)**

c. Explain and draw 4 bit Serial In / Parallel Out Shift Register, show the status of register at various clock pulses if data 10111 is fed into it. **(6)**