ROLL NO. _____

Subject: COMPUTER ORGANIZATION

Code: AC106/AT106

AMIETE - CS/IT {NEW SCHEME}

Time: 3 Hours

DECEMBER 2014

Max. Marks: 100

 (2×10)

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following:

a. The circuit used to store one bit of data is known as

(A)	Encoder	(B) Or gate
(C)	Flip Flop	(D) Decoder

b. Cache memory acts between

(A)	CPU and RAM	(B)	RAM and ROM
(C)	CPU and Hard Disk	(D)	None of these

c. Write through technique is used in which memory for updating the data

(A)	Virtual memory	(B) Main memory	
(C)	Auxiliary memory	(D) Cache memory	

d. Generally Dynamic RAM is used as main memory in a computer system as it

(A)	consumes less power	(B)	has higher speed
(C)	has lower cell density	(D)	needs refreshing circuitry

e. The circuit converting binary data in to decimal is

(A)	Encoder	(B)	Multiplexer
(C)	Decoder	(D)	Code converter

f. To reduce the memory access time we generally make use of _____.

(A)	Heaps	(B)	Higher capacity RAM's Cache's
(C)	SDRAM's	(D)	

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- g. MFC stands for,
 - (A) Memory Format Caches.
 - (C) Memory Find Command.
- (**B**) Memory Function Complete.
- (D) Mass Format Command.

h. The time delay between two successive initiation of memory operation _____.

- (A) Memory access time
- (B) Memory search time
- (C) Memory cycle time
- **(D)** Instruction delay
- i. In a vectored interrupt.
 - (A) the branch address is assigned to a fixed location in memory.
 - (B) the interrupting source supplies the branch information to the processor through an interrupt vector.
 - (C) the branch address is obtained from a register in the processor
 - (D) none of the above
- j. Von Neumann architecture is

(A)	SISD	(B)	SIMD
(C)	MIMD	(D)	MISD

Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

Q.2 a. Give a short sequence of machine instructions for the task: "Add the contents of memory location A to those of location B, and place the answer in location C".

Instructions

Load LOC, R_i

and

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Store R<sub>i</sub>, LOC
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are the only instructions available to transfer data between the memory and general purpose register R_i . (8)

- b. What are condition code flags? Explain any three commonly used flags. (2+6)
- Q.3 a. The subroutine call instruction of a computer saves the return address in a processor register called the link register, RL. What would you do to allow subroutine nesting? Would your scheme allow the subroutine to call itself? (8)

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	b. What do you understand by the data structures stack and queue? Explain how data is organized in computer memory as a stack? Also write two important differences between stack and groups implementation.	w it
	differences between stack and queue implementation.	(8)
Q.4	a. What do you understand by interrupt? What is the difference between subroutine and interrupt-service routine?	a (8)
	b. What is bus protocol? Also explain the difference between synchronous bus and Asynchronous bus.	d (8)
Q.5	a. Define I/O interface. What are the functions of an I/O interface?	(8)
	b. List out the various interface standards that may be used in computer system with the help of a diagram.	n (8)
Q.6	a. Explain the addressing scheme in computer memory. Also explain how dat transfer takes place between memory and processor.	a (8)
	b. Explain the designs of various Read-only memories.	(8)
Q.7	a. Explain with the help of a diagram virtual memory organization.	(8)
	b. A disk unit has 24 recording surfaces. It has a total of 14000 cylinders. There i an average of 400 sectors per track. Each sector contains 512 bytes of data.	S
	(i) What is the maximum number of bytes that can be stored in this unit?(ii) What is the data transfer rate in bytes per second at a rotational speed of 7200 rpm?	
	(iii) Using a 32-bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes per sector.	(8)
Q.8	a. Using manual methods, perform the operations $A \times B$ and $A \div B$ on the 5-bi unsigned numbers $A = 10101$ and $B = 00101$	it (8)
	b. State the rules of arithmetic operations on floating point numbers.	(8)
Q.9	a. Describe how a processor executes instructions. Explain it with the help of diagram?	a (8)
	b. Draw and explain the block diagram of a complete processor.	(8)

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