Code: AC103/AT103   Subject: ANALOG AND DIGITAL ELECTRONICS

AMIETE – CS/IT {𝒩𝓔𝓦 𝓢𝓒𝓗𝓔𝓜𝓔}

Time: 3 Hours   **DECEMBER-2014**   **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions selecting at least TWO from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1   Choose the correct or the best alternative in the following: (2×10)

a. The material used for forming P-type semiconductor is

   (A) Boron   **(B)** Arsenic
   (C) Phosphorous   **(D)** Antimony

b. The forward voltage drop across a practical silicon diode is

   (A) 0.3 V   **(B)** 0.7 V
   (C) 0.0 V   **(D)** Infinity

c. The average value of the half wave rectified output waveform is given by

   (A) 0.375 V_{PO} **(B)** 0.5 V_{PO}
   (C) 0.318 V_{PO} **(D)** 0.707 V_{PO}

d. The relationship between α_{DC} and β_{DC} is given by

   (A) $\beta_{DC} = \dfrac{1-\alpha_{DC}}{\alpha_{DC}}$ **(B)** $\alpha_{DC} = \dfrac{\beta_{DC}}{1-\beta_{DC}}$

   (C) $\beta_{DC} = \dfrac{\alpha_{DC}}{1-\alpha_{DC}}$ **(D)** $\alpha_{DC} = \dfrac{1-\beta_{DC}}{\beta_{DC}}$

e. The input and output resistances in a series voltage feedback are

   (A) Input resistance increases and output resistance decreases
   (B) Input resistance decreases and output resistance increases
   (C) Both input and output resistances decrease
   (D) Both input and output resistances increase

f. $(2AF)_{16} = (\quad)_{10}$

    (A) 687   **(B)** 667
    (C) 617   **(D)** 597

g. $\bar{x} + xy$

    (A) x   **(B)** $x + y$
    (C) $\bar{x} + y$ **(D)** $x + \bar{y}$

h. In a K-map, looping a quad of adjacent 1s eliminates

    (A) One variable   **(B)** Two variables
    (C) Three variables   **(D)** Four variables

i. 1's complement of 101101 is

    (A) 010011   **(B)** 010010
    (C) 100010   **(D)** 011100

j. In a Mod-8 counter, the output from the last flip-flop will have a frequency of
_____ of the input frequency

    (A) Half   **(B)** One fourth
    (C) One eighth   **(D)** One sixteenth

PART (A)
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Explain the formation of barrier voltage and depletion region in a PN junction.
                                                              (8)
    b. Explain the purpose of a dc load line. Write the equation for drawing a dc load
line for a series circuit consisting of a supply voltage (E), a resistor (R_1) and a
diode (D_1).   **(8)**

Q.3 a. Draw the circuit of two diode full wave rectifier and explain the working along
with the waveforms.   **(8)**

    b. Draw the positive and negative voltage clamping circuits. Explain its working
along with the waveforms.   **(8)**

Q.4 a. Explain the operation of PNP transistor with neat diagrams. Why they are
termed as 'bipolar' junction transistors?   **(8)**

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b. The base bias circuit shown in **Fig.1** has $R_B = 470k\Omega, R_C = 2.2k\Omega$ and $V_{CC} = 18V$, and the transistor has $h_{FE} = 100$. Determine I_B, I_C and V_{CE} **(8)**
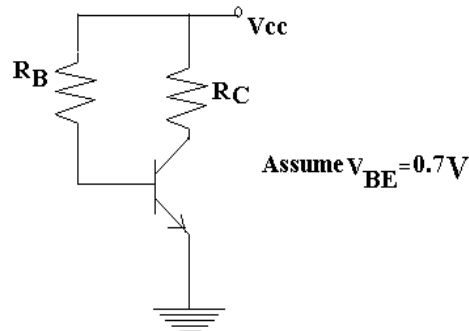

Fig.1

Q.5 a. Draw the circuit of single stage CE amplifier and explain the function of bypass capacitor and coupling capacitors. **(8)**

b. Explain the working of BJT phase shift oscillator with a neat circuit diagram. **(8)**

PART (B)
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Explain the parallel and serial transmission of information in digital systems. **(8)**

b. Explain the parity method for error detection. **(8)**

Q.7 a. Write DeMorgan's Theorems and simplify $z = \overline{(\overline{A} + C) \cdot (B + \overline{D})}$. **(8)**

b. Explain Exclusive – OR and Exclusive – NOR gates with neat diagrams. **(8)**

Q.8 a. Explain BCD adder with an example. **(8)**

b. What is a Demultiplexer? Explain with a diagram, the working of a 1 line to 8 line Demultiplexer. **(8)**

Q.9 a. Explain the working of a clocked J K flip flop with neat diagram and waveforms. **(8)**

b. Draw the diagram of a 4-bit Asynchronous Counter and explain its working along with the waveforms. **(8)**