ROLL NO. _____

Code: AE74 **Subject: VLSI DESIGN**

AMIETE – ET

Time: 3 Hours **DECEMBER 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The threshold voltage of p-MOS depletion mode transistor when V_{SB}=0 is

(A) V_{td}= +0.2V_{DD} **(B)** V_{td}= –0.7V_{DD}
(C) V_{td}= –0.2V_{DD} **(D)** V_{td}= +0.7V_{DD}

b. P-well CMOS fabrication process uses _____substrate

(A) P-type Semiconductor **(B)** N-type Semiconductor
(C) Pure conductor **(D)** Pure Insulator

c. The total number of transistors required to realize 4-input CMOS NAND gate is

(A) 4 **(B)** 16
(C) 8 **(D)** 10

d. If V_{tn}=+0.5V and V_{in1}= V_{in2} =2.9V then the output voltage (V_{out}) of the n-FET structure shown in figure1 is

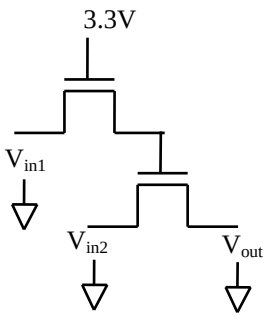

Figure1

(A) 2.3V **(B)** 2.9V
(C) 3.3V **(D)** 0V

e. In n-MOS design rules the minimum separation between poly silicon to diffusion is

(A) 2λ **(B)** 1λ
(C) 3λ **(D)** 4λ

f. In 5μm technology, if a metal length is 30λ, width is 4λ and metal to substrate relative C value is $0.075 \square C_g$ then its capacitance with respect to substrate is

(A) $4 \square C_g$ **(B)** $2.25 \square C_g$
(C) $1.125 \square C_g$ **(D)** $1 \square C_g$

g. _____ are used to join metal1 to metal 2 layers

(A) Simple contacts **(B)** Buried contacts
(C) Vias **(D)** Butting contacts

h. In a CMOS inverter with equal length of PMOS and NMOS transistors the rise time and fall time will be equal when

(A) $W_p=W_n$ **(B)** $W_p=2.5W_n$
(C) $2.5W_p=W_n$ **(D)** $W_p=5W_n$

i. In constant voltage scaling model, the gate capacitance (C_g) is scaled by

(A) $\frac{1}{\alpha^2}$ **(B)** $\frac{1}{\beta^2}$
(C) $\frac{\beta}{\alpha^2}$ **(D)** $\frac{1}{\alpha}$

j. The propagation delay of cascaded pass transistors is given by

(A) $rc\tau$ **(B)** $2.5ne\tau$
(C) $n^2rc\tau$ **(D)** $3.5ne\tau$

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain with sketches n-well process of CMOS fabrication. **(8)**

b. What are the advantages of E-beam masks? Explain the steps involved in making E-beam mask. **(8)**

Q.3 a. Derive an expression for Pull-up to Pull-down ratio for an n-MOS inverter driven through one or more pass transistors. **(8)**

b. Draw BiCMOS inverter circuit with MOS transistors for base current discharge and explain its operation. **(5)**

c. An inverter uses FETs with β_n=2.1mA/V^2 and β_p=1.8mA/V^2, the threshold voltages are given as V_{tn}=0.6V, V_{tp}=-0.7V and a supply voltage of V_{DD}=5V. Calculate midpoint voltage. **(3)**

Q.4 a. Discuss λ-based C-MOS design rules for P-well and contacts. **(8)**

b. Draw the monochrome stick encoding of **(8)**
(i) 2-input CMOS NOR gate
(ii) Two-way selector with enable

Q.5 a. Obtain the expression for total delay for N stages of NMOS and CMOS inverters in terms of width factor 'e' and delay factor 'τ'. **(8)**

b. Define sheet resistance and standard unit of capacitance $\square C_g$. Find the static and dynamic resistance of a minimum sized CMOS inverter. **(8)**

Q.6 a. Write the scaling factors for the following device parameters: **(8)**

(i) Saturation current I_{dss} (ii) Channel resistance R_{on}
(iii) Gate delay (iv) Power speed product (P_T)

b. Explain the structured design of a parity generator with necessary blocks and write stick diagram of a NMOS one bit parity generator cell. **(8)**

Q.7 a. What are the problems associated with the design of VLSI system. How to overcome these problems? **(5)**

b. Draw and explain carry-select adder (6-bit) structure. **(8)**

c. Write Manchester carry-chain element and explain its operation. **(3)**

Q.8 a. Explain with circuit diagram:-

(i) Six transistor static CMOS memory cell
(ii) CMOS pseudo-static D-flipflop **(5+5)**

b. Explain the optimization of NMOS inverter. **(6)**

Q.9 Write short notes on: **(4×4=16)**

(i) System partitioning
(ii) Design testability
(iii) Testing of combinational logic
(iv) Boundary Scan Test (BST)