ROLL NO. _____

Code: AE68 Subject: EMBEDDED SYSTEMS DESIGN

AMIETE – ET

Time: 3 Hours **DECEMBER 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. In Embedded System, market window often measured in

(A) Years **(B)** Months
(C) Days **(D)** Both **(A)** & **(B)**

b. The time between the start of the task's execution and the end is called

(A) Response Time **(B)** Latency
(C) Execution Time **(D)** Both **(A)** & **(B)**

c. The disadvantage of ASIP in an embedded system is

(A) Performance **(B)** NRE Cost
(C) Power and Size **(D)** None of these

d. The advantages of Mask-Programmed ROM are

(A) Density **(B)** Speed
(C) Low Write Ability **(D)** All of these

e. UART

(A) Receive data serially and store serially
(B) Receive data serially and store parallely
(C) Receive data parallely and store serially
(D) Receive data Parallely and store parallely

f. A single chip with multiple processors is often referred to as a

(A) Multi-core chip **(B)** ASIC
(C) SOC **(D)** FPGA

g. The Debuggers run on the

(A) Development Processor **(B)** System Processor
(C) Target Processor **(D)** Both **(A)** & **(C)**

h. A measure of the number of bits that are sent over a connection in a one second is called

(A) Baud Rate **(B)** Bit Rate
(C) Both Bit & Baud Rate **(D)** None of these

i. The FPM DRAM is

(A) Fast Page Mode DRAM
(B) Ferro Page Mode DRAM
(C) Full Programmable Mode DRAM
(D) None of these

j. A cache line also known as:

(A) Cache offset **(B)** Cache block
(C) Cache hit **(D)** Cache miss

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. List and define the three main characteristics of embedded systems that distinguish such systems from other computing systems. Draw and explain the simplified revenue model for computing revenue loss from delayed entry of the embedded product to market. **(8)**

b. What is a "market window" and why is it so important for products to reach the market early in this window? **(8)**

Q.3 a. Compare the following: **(8)**
(i) Superscalar and VLIW architectures
(ii) Princeton and Harvard

b. Explain the main features of Timers, Counters and Watchdog Timers. **(8)**

Q.4 a. Explain how a PC communicates serially with an embedded device. Describe transmission protocol used by the two UARTs. **(8)**

b. Draw the internal view of an 8 x 4 ROM and explain the ROM main features. **(8)**

Q.5 a. Compare Fixed and Vectored interrupts. **(6)**

b. Interface 8k of data and 32k of program code memory to an 8051 microcontroller. Explain how a memory read operation performs. **(10)**

Q.6 a. Explain different addressing modes used to indicate the data's location in assembly language programming. **(8)**

b. Explain the concept of scheduler in RTOS in detail with example. **(8)**

Q.7 a. Explain Shared Data Problems and Re-entrant functions in RTOS. **(8)**

b. Explain the RTOS memory management subsystem. **(8)**

Q.8 a. Describe the architecture of basic DRAM and also explain advanced DRAM with suitable diagrams. **(8)**

b. With the help of an example & diagram define heartbeat timer in detail. **(8)**

Q.9 a. List the advantages and disadvantages of using a large number of tasks. **(8)**

b. How messages passed through the RTOS in Telegraph Operation and how it deals with an interrupt routine. **(8)**