ROLL NO. _____

Code: DE60/DC68/DE111/DC111
Subject: MICROPROCESSORS & MICROCONTROLLERS

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. When the control unit (CU) of 8085 sends a logic 0 on RD* pin it indicates that it reads information from _____.
(A) AD7-AD0 **(B)** A15-A8
(C) AD15-AD0 **(D)** None of these

b. In ADI D8 instruction, ADI stands for
(A) Add Immediate to accumulator **(B)** Add Instruction to accumulator
(C) Address to accumulator **(D)** Add to accumulator

c. RIM is used to check whether.
(A) The write operation is done
(B) The interrupt is masked or not
(C) The read operation is done or not
(D) Both **(A)** & **(B)**

d. In 8085, example of non maskable interrupt
(A) TRAP **(B)** RST
(C) INTR **(D)** RST 5.5

e. When DMA transfer is performed, Processor goes to ____ state and gives up control of the _____ BUS.
(A) HOLD, system **(B)** Active, address bus
(C) Slave, Data bus **(D)** Master, system bus

f. CMP M instruction of 8085 means
(A) Complement the memory data
(B) Complement the carry flag
(C) Compare memory with accumulator
(D) Compare if minus

g. Which data transfer scheme is fastest among the following
(A) Programmed I/O **(B)** DMA
(C) Serial I/O **(D)** None of these

h. Which interrupt has the lowest priority among the following interrupts.
(A) TRAP **(B)** RST 7.5
(C) RST 6.5 **(D)** INTR

i. XTHL instruction exchanges the contents of top two locations of stack with the contents of which register pair.
(A) BC **(B)** HL
(C) DE **(D)** AF

j. When CALL instruction is executed the return address is stored on
(A) Memory **(B)** Accumulator
(C) Top of stack **(D)** None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Briefly describe programmer's view of 8085 and need for accumulator. **(4)**

b. Explain the following set of instructions with the help of one example of each. **(12)**
(i) LDA a16
(ii) MOV r, M
(iii) MVI M, d8
(iv) XCHG
(v) LHLD a16
(vi) STAX r_p

Q.3 a. Differentiate between unconditional and conditional branch instructions, mention various conditional call instructions. **(4)**

b. With a neat block diagram, explain the architecture of 8085. **(12)**

Q.4 a. Write an 8085 assembly language program and flow chart to search for a given byte in an array of bytes using linear search algorithm. Location X contains the size of the array and location X + 1 contains the element to be searched. The elements of the array are stored from location Y onwards. The program should display in the address field, the search element and the position when it was found. If the search element is not found, the position should be indicated as 00. **(8)**

b. Write an 8085 assembly language program and flowchart to exchange 10 byte of data stored from location X with 10 byte of data stored from location Y. **(8)**

Q.5 a. Mention different data transfer schemes to communicate with a I/O device and explain any one scheme in detail. **(12)**

b. Write the action taken by 8085 when INTR pin is activated. **(4)**

Q.6 a. Explain Port C bit set/reset control word of 8255. Write the required Port C bit set/reset control word for each of the following cases- **(12)**

(i) To reset to 0 bit 5 of Port C
(ii) To set to 1 bit 3 of Port C

b. Write the functional pin diagram of Intel 8279 **(4)**

Q.7 a. Explain all the registers used in 8259 **(8)**

b. What is DMA? Explain the need for DMA data transfer. **(4)**

c. Mention the conditions for the following modes w.r.t.8257

(i) When processor is the master & 8257 is slave.

(ii) When processor is in HOLD stack & 8257 is in master mode **(4)**

Q.8 a. Explain the internal architecture of 8253. **(8)**

b. Discuss the following w.r.t. 8251

(i) Asynchronous Transmission

(ii) Synchronous Transmission **(8)**

Q.9 a. Mention the salient features and functional pin diagram of INTEL 8051. **(8)**

b. Explain the following instruction of 8051 **(8)**

(i) MOVXA, @ DPTR
(ii) CLR C
(iii) DIV A B
(iv) XCHD A, @ R1