ROLL NO. _____

Code: DE58/DC58/DE108/DC108 **Subject: LOGIC DESIGN**

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The number of bits in ASCII code is _____
(A) 12 **(B)** 9
(C) 10 **(D)** 7

b. The 8421 BCD equivalent of Hexadecimal number FF_{16} is_____
(A) 0000 0101 0101 **(B)** 0010 0101 0101
(C) 1111 0101 0101 **(D)** 1000 0101 0101

c. DeMorgan's second theorem is _____
(A) $A.\overline{A} = 0$ **(B)** $\overline{\overline{A}} = A$
(C) $\overline{A+B} = \overline{A}.\overline{B}$ **(D)** $\overline{AB} = \overline{A}.\overline{B}$

d. A Karnaugh map with 4 variables has _____
(A) 2 cells **(B)** 8 cells
(C) 4 cells **(D)** 16 cell

e. In a D latch _____
(A) data bit D is fed to S input and $\overline{D}$ to R input
(B) data bit D is fed to R input and $\overline{D}$ to S input
(C) data bit D is fed to R and S inputs
(D) data bit $\overline{D}$ is not fed to any input

f. When two 4-bit parallel adders are cascaded we get _____
(A) 4-bit parallel adder **(B)** 8-bit parallel adder
(C) 16-bit parallel adder **(D)** 32-bit parallel adder

g. A 4-bit down counter can count from _____
(A) 0000 to 1111 **(B)** 1111 to 0000
(C) 0101 to 1111 **(D)** 111 to 000

h. In a 7 segment display, LEDs a,b and c light up. The decimal number displayed is _____
(A) 9 **(B)** 3
(C) 7 **(D)** 1

i. An 8 bit data is to be entered into a parallel in register. The number of clock pulses require is _____
(A) 8 **(B)** 2
(C) 4 **(D)** 1

j. The memory does not require programming equipment is_____
(A) RAM **(B)** EEPROM
(C) EPROM **(D)** UVPROM

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is a Digital System? Explain the advantages and limitations of Digital Techniques over Analog Techniques. **(8)**

b. Convert the decimal number 82.67 to its equivalent binary number. **(4)**

c. Explain the five functional units of a computer. **(4)**

Q.3 a. Simplify the logic expression F = $\overline{ABC} + \overline{AB}\,C + \overline{A}\,B\,\overline{C} + A\,\overline{BC} + A\,\overline{B}\,C$ using boolean algebraic theorems. **(6)**

b. Draw the logic diagram for 4-bit Even Parity Generator and explain its operation. **(4)**

c. Minimize the logic function F(A, B, C, D) = $\sum$ m(1,3,5,8,9,11,15) + d(2,13) using K-maps. **(6)**

Q.4 a. What is a Flip-Flop? Draw the logic diagram for Master Slave Flip-Flop and explain its function with the help of truth table. **(8)**

b. Explain the application of Flip-Flop as a Shift Register using D Flip-Flops. **(8)**

Q.5 a. (i) Perform the Addition of -20 to +26 using 2's complement System. **(4)**
(ii) Perform the Subtraction of 0011.1001- 0001.1110 using 2's Complement System. **(4)**

b. What is the need of Parallel Binary Adder? Draw the block diagram of four-bit Parallel Adder using Full Adders and explain its operation. **(8)**

Q.6 a. What is a Ripple Counter? Draw the logic diagram of 3-bit Ripple Counter and explain its working with the help of timing diagram. **(8)**

b. What is Synchronous Counter? Draw the logic circuit of MOD 8 Synchronous Counter and explain its working with timing waveform. **(8)**

Q.7 a. What is Magnitude Comparator? Explain 2-bit Magnitude Comparator with the help of truth table. **(9)**

b. What is an Encoder? Draw the truth table for 10-line Decimal to 4-line BCD Encoder and implement the logic diagram from the truth table. **(7)**

Q.8 a. Design a MOD-6 Synchronous Counter and draw its designed logic diagram. **(9)**

b. Draw the logic diagram for 4-bit Serial Input and Serial Output Shift Register and explain its working with timing waveform. **(7)**

Q.9 a. Draw and explain the architecture of 16 X 8 ROM. **(10)**

b. Differentiate between Static RAM and Dynamic RAM. **(6)**