ROLL NO. _____

Code: CT76 **Subject: MICROELECTRONICS AND VLSI DESIGN**

ALCCS

Time: 3 Hours DECEMBER 2015 **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Why MOS technology has become dominant technology in IC industry?

b. What is the use of SiO_2 layer in MOSFET devices?

c. Draw the graph of V_{GS} and I_{DS}, for a fixed V_{DS} of p-channel & n-channel depletion transistors.

d. List the all second order effects of MOSFET.

e. With the help of example, explain Mealy and Moore machine.

f. List all the Sources of Power Dissipation in MOS devices.

g. List the electrical faults in turn can be translated into logical faults **(7x4)**

Q.2 a. Explain the enhancement mode MOS transistor action. **(4)**

b. Explain with neat sketch, Bridgman Technique of crystal growth. **(8)**

c. Calculate the threshold voltage V_{TO} at V_{SB} = 0 for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping $N_A = 10^{16}cm^{-3}$, polysilicon gate doping density $N_D = 2\times10^{20}cm^{-3}$, gate oxide thickness $t_{ox} = 500\,\mathring{A}$ and oxide interface fixed charge density $N_{OX} = 4\times 10^{10}cm^{-2}$. **(6)**

Q.3 a. Draw and explain Schematic, Stick Diagram and Layout of n-MOS depletion load inverter. **(10)**

b. Explain the wafer shaping techniques used after crystal growth. **(8)**

Q.4 a. Define port mode of the interface and describe all Port modes of an Entity. **(6)**

b. What is a Process? Explain the process block execution of statements. **(8)**

c. Write a behavioural modelling of one-bit comparator. **(4)**

Q.5 a. Discuss the Limitations of Scaling in VLSI Designs. **(8)**

b. Explain Structured Design Approach – Regularity with example. **(10)**

Q.6 a. Write the circuit of one transistor dynamic RAM cell and explain briefly read and write functions. **(10)**

b. Explain the optimization of CMOS Inverters. **(8)**

Q.7 a. Explain different aspects of CAD Design Tools. **(8)**

b. Explain Advantages & Disadvantages of implementing BIST include. **(10)**