ROLL NO. _____

Code: CT12 **Subject: COMPUTER ARCHITECTURE**

ALCCS

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. What do you understand by the term Computer organization, design and architecture?

b. Explain the differences between hardwired and Micro-programmed control unit.

c. Explain the instruction pipelining in the RISC processor.

d. What is the maximum positive and negative value if number is represented using 8 bits including the sign bit in
(i) signed magnitude representation
(ii) 1's complement representation and
(iii) 2's complement representation

e. What is the stack memory and what is the roll of stack in subroutine?

f. A computer system uses the memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation cjode, a register code part to specify one of 64 registers, and an address part. Draw the instruction format and indicate the number of bits in each part

g. Draw the memory hierarchy system. Clearly mention the speed, capacity and access type at each level of memory hierarchy. **(7 × 4)**

Q.2 a. Draw the block diagram of Wallace tree multiplier to multiply two 4-bit numbers. Explain the operation performed by multiplier with example. **(9)**

b. An instruction of computer system has two parts: Op-code and Operand. Instruction is stored at two consecutive locations of memory as given below. It has one general purpose register (R1) and index register (XR). Content of memory with their addresses are given below. Contents of Register R1 and index register XR are 400 and 100 respectively. What will be value of AC after the execution of instruction, in following addressing modes? **(9)**

(i) Register addressing mode.
(ii) Immediate addressing.
(iii) Direct Addressing
(iv) Indirect Addressing
(v) Register indirect
(vi) Indexed Addressing

Addr.	***Contents***
200	*Load to AC*
201	*500*
:	
399	*450*
400	*700*
:	
500	*800*
:	
600	*900*
:	
702	*325*
:	
800	*800*

Q.3 a. What are the steps required for data transfer using DMA controller? Explain the interfacing diagram of DMA controller with computer system. **(9)**

b. A computer has the memory capacity of 2048 x 16. It is based on the micro-programmed control unit. Size of control memory is 128 x 20. Draw the block diagram of micro-program sequencer for given computer. **(9)**

Q.4 a. What do you understand by general register organised CPU? Draw the block diagram of bus organization for general register organized CPU, which has following control word (instruction format).

SEL A	SEL B	SEL D	ORP
(3 bits)	(3 bits)	(3 bits)	(5 bits)

Where SEL A and SEL B are two source register and SEL D is destination register field. ORP is 5-bit operation code field. **(9)**

b. Explain the IEEE-754 single precision floating point representation and its format. Represent -1.5_{10} in single precision IEEE-754 floating-point representation. **(9)**

Q.5 a. How mapping from an instruction code to microinstruction address is being performed by Control Address Register? Explain the mapping procedure with suitable diagram. **(9)**

b. Design an arithmetic circuit to generate the following arithmetic operations. Draw the logic diagram of one typical stage. **(9)**

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = \overline{B} + A$	$F = \overline{B} + A + 1$
1	0	$F = A$	$F = A + 1$
1	1	$F = A - 1$	$F = A$

Q.6 a. A digital computer has a memory unit of 64K x 16 and a cache memory of 1K word. The cache uses direct mapping with a block size of four words.
(i) How many bits are there in the tag, index, block and word field of the address format?
(ii) How many bits are there in each word of cache, and how are they divided in to functions?
(iii)How many blocks can the cache accommodate? **(9)**

b. Explain the isolated (peripheral) mapped I/O and memory-mapped I/O. What are the advantages and disadvantages of each? **(9)**

Q.7 a. What is parallel processing and what are the different levels of parallel processing? How parallelism can be achieved in uni-processor system? **(9)**

b. Describe the classification of parallel computer. Draw the block diagram and explain each classification. **(9)**