ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. CMOS is equal to

(A) NMOS+ PMOS **(B)** PMOS+PMOS
(C) VMOS+NMOS **(D)** None of the above

b. To achieve equal pullup and pulldown times in a CMOS inverter, the P device is usually several times wider than the N device. What is the main reason for this?

(A) Hole mobility is greater than electron mobility.
(B) Electron mobility is greater than hole mobility.
(C) The P threshold is greater than the N threshold.
(D) The N threshold is greater than the P threshold.

c. Which of the following layers is NOT needed to layout an nMOS transistor?

(A) Active **(B)** Via
(C) Poly **(D)** n-Select

d. In saturation mode of operation drain current I_{ds} depends on

(A) $V_{GS,}V_t$ **(B)** V_{DS},V_{GS},V_{SB}
(C) V_{GS} **(D)** None of the above

e. Which equation is correct? V_{NL} = Noise Margin Low, V_{NH} = Noise Margin High

(A) $V_{NL} = V_{IL(max)} + V_{OL(max)}$ **(B)** $V_{NH} = V_{OH(min)} + V_{IH(min)}$
(C) $V_{NL} = V_{OH(max)} - V_{IH(max)}$ **(D)** $V_{NH} = V_{OH(min)} - V_{IH(min)}$

f. Which logic family combines the advantages of CMOS and TTL?

(A) BiCMOS **(B)** TTL/CMOS
(C) ECL **(D)** TTL/MOS

g. The total propagation delay time T in Carry Skip Adder is given by

(A) $T = n/M$ **(B)** $T = 2 (P–1) K_1 + (M–2) K_2$
(C) $T = 2 (P–1) K_1$ **(D)** $T = M/n$

h. The power consumption is least in CMOS circuits as compared to NMOS and PMOS circuits. This is because, in CMOS
(A) Both the transistors remain in off-state most of the time.
(**B)** Small voltages are required.
(C) High value resistors are used
(D) Both the transistors go to on-state simultaneously only for a very short time during change of states

i. The gate area of the device is

(A) $A_g = C_{ox} L W$ **(B)** $A_g = L W$

(C) $A_g = LW/C_{ox}$ **(D)** $A_g = C_o L$

j. The fastest memory is

(A) DRAM **(B)** ROM
(C) CACHE **(D)** EPROM

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the C-V characteristics of Ideal MOS System. Explain Flat Band Voltage. **(8)**

b. Explain the different fabrication steps of n well process for CMOS Inverter. **(8)**

Q.3 a. Derive the expression for the threshold voltage of a MOS transistor and explain the significance of different parameters present in the equation. **(8)**

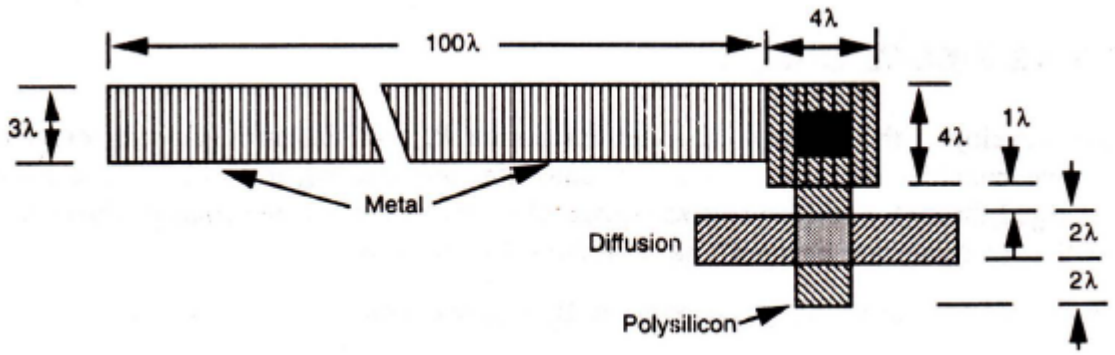
b. Determine the pull up to pull down ratio for an n MOS inverter driven through one or more pass transistors. **(8)**

Q.4 a. Draw the schematic for EX-OR gate using CMOS logic. **(8)**

b. Explain Lambda (λ) based design rules. **(8)**

Q.5 a. Explain how to estimate wiring capacitances? **(8)**

b. Calculate area capacitance values associated with structures occupying more than one layer as shown in figure given below **(8)**



Typical area capacitance values for MOS circuits

Capacitance	*Value in pF × 10^{-4}/μm² (Relative values in brackets)*		
	5 μm	*2 μm*	*1.2 μm*
Gate to channel	4 (1.0)	8 (1.0)	16 (1.0)
Diffusion (active)	1 (0.25)	1.75 (0.22)	3.75 (0.23)
Polysilicon* to substrate	0.4 (0.1)	0.6 (0.075)	0.6 (0.038)
Metal 1 to substrate	0.3 (0.075)	0.33 (0.04)	0.33 (0.02)
Metal 2 to substrate	0.2 (0.05)	0.17 (0.02)	0.17 (0.01)
Metal 2 to metal 1	0.4 (0.1)	0.5 (0.06)	0.5 (0.03)
Metal 2 to polysilicon	0.3 (0.075)	0.3 (0.038)	0.3 (0.018)

Notes: Relative value = specified value/gate to channel value for that technology.
*Poly. 1 and Poly. 2 are similar (also silicides where used).

Q.6 a. What is short channel effect? Explain **(8)**

b. Explain the difference between static Logic circuits and Dynamic Logic Circuits **(8)**

Q.7 a. Design and explain 4 X 4 crossbar switch. **(8)**

b. Draw and explain a possible arrangement of the adder elements for both arithmetic and logical functions. **(8)**

Q.8 a. Briefly explain the operation of 6T SRAM memory structure with read and write circuitry. Explain their timing diagrams. **(8)**

b. Discuss the different ground rules for successful design. **(8)**

Q.9 a. Explain the aspects of design tools. **(8)**

b. Explain different VLSI design styles. **(8)**