ROLL NO. _____

Code: AE68/AE117 Subject: EMBEDDED SYSTEMS DESIGN

AMIETE – ET (Current & New Scheme)

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. An embedded system has RAM memory

(A) For storing the variables during program run, stack and input or output buffers, for example, for speech or image
(B) For storing all the instructions and data
(C) For storing the programs from external secondary memory
(D) For fetching instructions and data into cache

b. (i) A compiler generates an object file.
(ii) The object file is linked with library functions using linker.
(iii) After re-allocation of addresses a locator sends the codes to device programmer for burning as ROM image in embedded system ROM.
(iv) After re-allocation of addresses a loader loads the codes to device programmer for burning as ROM image in embedded system ROM.
(v) After re-allocation of addresses a loader loads the codes in RAM.
Steps for embedded system development are:

(A) i, ii and iv **(B)** i, iii, iv and v
(C) i, ii and iii **(D)** i, ii, iv and v

c. A device driver is software for

(A) Upgrading the operating systems
(B) Receiving input or sending outputs from device
(C) Access to parallel or serial port by the device
(D) Controlling the device for communication with hardware

d. Design metrics are

(i) engineering cost (ii) time to market
(iii) power dissipation (iv) flexibility
(v) system and user safety (vi) performance
(vii) prototype development time (viii) maintenance of the system

(A) All **(B)** All except v and viii
(C) iii and vi **(D)** All except i and ii

e. A communication protocol specifies
(i) the ways of communication of signals on the bus
(ii) ways of arbitration when several devices need to communicate through the bus or the ways of polling from the devices need of the bus at an instance
(iii) memory requirement during communication
(iv) minimum rate of data transfer during communication
(v) interrupt service mechanism

(A) i, ii, iii and iv **(B)** i, iii, iv and v
(C) i and ii **(D)** i, ii and iii

f. Total power dissipation can be reduced by
(i) reducing operating voltages,
(ii) operating at lower clock frequency if processes meet the deadlines
(iii) use of wait and stop instructions when system is inactive or idle
(iv) use of cache disabling instructions
(v) optimizing the amount and type of hardware required for the system

(A) All except v **(B)** i, ii and iii
(C) All except iv **(D)** All

g. In the following subroutine, the goal is to return true if and only if the input is a number 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, or 0x39.

```
longCheckInput(long input)
{
if ((input  xxx  0X30 )  yyy  (input  zzz  0x39))
return 1;  // true
else
return 0;  // false
}
```

What C code do you need to place in the xxx, yyy, zzz position of the program to return the true?

(A) ==, &&, == **(B)** >=, &&, <=
(C) >=,||,<= **(D)** ==, ||, ==

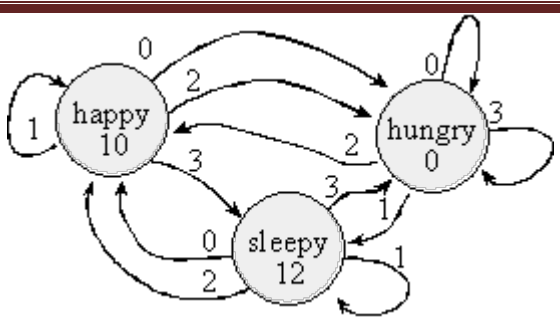
h. An 8-bit ADC has an input range of 0 to +10 volts and an output range of 0 to 255 (called straight binary). What digital value will be returned when an input of +7.5 volts is sampled? Give your answer as a decimal number.

(A) 191
(B) 192.3
(C) 192
(D) 193

i. Which one of these is not a serial protocol

(A) I^2C **(B)** CAN
(C) Fire Wire **(D)** ARM

j. In the FSM below, assume we start in the happy state. The input starts and remains 3. What sequence of outputs will occur?



(A) start and remain at 0
(B) 10, 12, 0 (and remain at 0)
(C) 10, 0, 10, 0, 10, 0, 10, 0, 10, over and over
(D) 10, 12, 10, 12, 10, 12, 10, 12, 10, over and over

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Discuss design metrics and explain with an example how metrics typically compete with each other. **(5)**

b. What are the IC Technology available for digital circuit implementation? Explain the current state of art for this. **(5)**

c. Design process of a chip is itself quite complex and is constantly evolving. Discuss the steps in Design process and give an example of how it is being improved. **(6)**

Q.3 a. Differentiate between timer, counter and watchdog Timer. **(3)**

b. Given a timer structured with 16 bit up counter and a clock frequency of 10 MHz, determine its range and resolution. **(4)**

c. Explain Pulse With Modulation Modulators with help of an example showing control of a DC motor using PWM technique**.** **(9)**

Q.4 a. What benefits are derived if we choose to implement systems functionality on a general purpose processor? **(4)**

b. Define (i) MIPS (ii) throughput (iii) benchmarks with examples **(3)**

c. What forms the programmers view of a processor? Give the fields that form part of an instruction. Explain with the help of an example. **(3)**

d. Discuss the various addressing modes possible in a processor. **(6)**

Q.5 a. Explain and Compare direct mapping and fully associative mapping for Cache mapping. **(4)**

b. A given design with cache implemented has a main memory access cost of 20 cycles on a miss and two cycles on a hit. The same design without the cache has a main memory access cost of 16 cycles. Calculate the minimum hit rate of the cache to make the cache Implementation worthwhile. **(8)**

c. Define and discuss NVRAM. **(4)**

Q.6 a. Discuss the classification of port based and bus based I/O with further sub-classification details. **(4)**

b. Discuss multilevel bus architectures with the help of an industry standard multilevel bus. **(4)**

c. Discuss the IEEE 802.11 protocol standard for bus communication. What are the protocols for wireless communication? **(8)**

Q.7 a. Define Tasks and Task States. **(4)**

b. What is a re-entrant function? What are its characteristics? What are the grey areas in re-entrancy? Explain with example. **(6)**

c. When is a task blocked? What are the common issues of task state which are dealt by scheduler? **(6)**

Q.8 a. What is the basic task of queues mailboxes and pipes? Explain with an example how they help to improve execution time? What decides the choice from amongst them? **(6)**

b. What issues are involved in using queues in an RTOS? **(4)**

c. How is INTERRUPT ROUTINE code different from Task Code? For an INTERRUPT ROUTINE explain with a suitable example as to how it should work in an RTOS? **(6)**

Q.9 a. How do we select the optimum number of tasks a system work should be divided into? **(6)**

b. Give the pseudo code for a Task structure. Explain the pros and cons of it. **(5)**

c. Saving memory and power are critical to an embedded system. Discuss methods for saving power in an embedded system. **(5)**