ROLL NO. _____

Code: AE54/AC54/AT54/AE104 **Subject: LINEAR ICs & DIGITAL ELECTRONICS**

AMIETE – ET/CS/IT (Current & New Scheme)

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

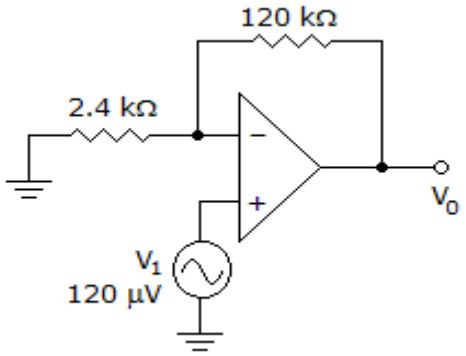
PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The output voltage V_0 for the circuit shown below:



(A) -6.00 mV **(B)** 6.00 mV
(C) -6.12mV **(D)** 6.12Mv

b. CMRR of ideal opamp is _____

(A) 0 **(B)** 1
(C) infinity **(D)** finite

c. The ratio of change in input offset voltage when variation in supply voltage is made known as _____

(A) PSRR **(B)** CMRR
(C) OSRR **(D)** input offset variation

d. What is the function of the comparators in the 555 timer circuit?

(A) To compare the output voltages to the internal voltage divider
(B) To compare the input voltages to the internal voltage divider
(C) To compare the output voltages to the external voltage divider
(D) To compare the input voltages to the external voltage divider

e. R-2R Converter is _____

(A) DC to AC **(B)** Analog to digital
(C) Digital to analog **(D)** None of these

f. How many flip flops are required to construct a decade counter _____

(A) 10 **(B)** 4
(C) 3 **(D)** 2

g. DeMorgan's first theorem shows the equivalence of _____

(A) OR gate and Exclusive OR gate. **(B)** NOR gate and Bubbled AND gate.
(C) NOR gate and NAND gate. **(D)** NAND gate and NOT gate

h. The 2's complement of the number 1101101 is _____

(A) 0101110 **(B)** 0111110
(C) 0110010 **(D)** 0010011

i. The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either _____

(A) a NAND or an EX-OR **(B)** an OR or an EX-NOR
(C) an AND or an EX-OR **(D)** a NOR or an EX-NOR

j. The number of control lines for 8 to 1 multiplexer is _____

(A) 1 **(B)** 2
(C) 3 **(D)** 4

PART A
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Draw the inverting Operational amplifier and derive the expression for the voltage gain. **(10)**

b. Explain the ideal characteristics of operational amplifier. **(6)**

Q.3 a. Define slew rate, input offset voltage, input bias current and input offset current of the operational amplifier. **(8)**

b. Draw and explain the voltage to current converter circuit using operational amplifier. **(8)**

Q.4 a. Draw and explain the ideal integrator circuit by deriving the suitable expression. **(8)**

b. Explain the operation of sample & hold circuit. Discuss its applications. **(8)**

Q.5 a. What is an ADC? Draw the schematic of an ADC that uses a binary counter and explain its operation. **(8)**

b. Explain with suitable circuit diagram the working principle of monostable-multivibrator circuit operation using IC 555. **(8)**

PART B
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Enlist the advantages of digital system over analog. **(6)**

b. (i) What is the total range of decimal values that can be represented in eight bits?

(ii) How many bits are needed to represent decimal values ranging from 0 to 12,500? (**4**)

c. Make the following conversion (steps are necessary): **(6)**

(i) $(874)_{10}$ to BCD
(ii) 0110100000111001 (BCD) to its decimal equivalent.
(iii) $(2AF)_{16}$ to decimal

Q.7 a. Simplify the following : **(6)**
(i) $\overline{A}BCD + ACD$ (ii) $(\overline{A} + B)(A + B)$

b. Minimize the logic function F (A, B, C, D) = $\sum m(1,3,5,8,9,11,15) + d(2,13)$ using K-maps and realize using NAND gates. **(10)**

Q.8 a. What is a half-adder? Explain a half-adder with the help of truth-table and logic diagram. **(8)**

b. What is a digital multiplexer? Illustrate its functional diagram. Write the scheme of a 4-input multiplexer using basic gates (AND/OR/NOT) and explain its operation. **(8)**

Q.9 a. With the help of clocked JK flip flops and waveforms, explain the working of a three bit binary ripple counter. **(8)**

b. Using D-Flip flops and waveforms explain the working of a 4-bit SISO shift register. **(8)**