ROLL NO. _____

Code: AE53/AC53/AT53/AE103 Subject: ELECTRONIC DEVICES & CIRCUITS

AMIETE – ET/CS/IT (Current & New Scheme)

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The solid state devices in electronic circuits are modelled by dependent sources and _____.

(A) Active elements **(B)** Passive elements
(C) Independent sources **(D)** None of these

b. Zener diode is _____

(A) Heavily doped **(B)** lightly doped
(C) Moderately doped **(D)** Undoped

c. For the BJT to operate in the active (linear) region the base-emitter junction must be _____-biased and the base-collector junction must be _____-biased.

(A) forward, forward **(B)** forward, reverse
(C) reverse, reverse **(D)** reverse, forward

d. In a Forward Biased PN junction diode, the sequence of events that best describes the mechanism of current flow is _____

(A) Injection and subsequent diffusion and recombination of minority carriers.
(B) Injection and subsequent drift and generation of minority carriers.
(C) Extraction and subsequent diffusion and generation of minority carriers.
(D) Extraction and subsequent drift and recombination of minority carriers.

e. How many semiconductor layers are thyristors constructed with?

(A) 2 **(B)** 3
(C) 4 **(D)** 5

f. In the Wien bridge oscillator, which of the following is (are) frequency-determining components?

(A) R1 and R2 **(B)** C1 and C2
(C) R1, R2, C1, and C2 **(D)** None of these

g. Internal transistor junction capacitances affect the high-frequency response of amplifiers by

(A) reducing the amplifier's gain.
(B) introducing phase shift as the signal frequency increases.
(C) having no effect
(D) both option **(A)** & **(B)**

h. The most stable biasing technique used is the _____

(A) voltage-divider bias **(B)** base bias.
(C) emitter bias. **(D)** collector bias.

i. Which type of power amplifier is biased for operation at less than 180º of the cycle?

(A) Class A **(B)** Class B
(C) Class C **(D)** Class D

j. A BJT is a:

(A) current controlled & bipolar device
(B) voltage controlled device & bipolar device
(C) current controlled & Unipolar device
(D) voltage controlled device & Unipolar device

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. By using Norton's theorem, find the current in the load resistor R_L for the circuit shown in Fig.1. **(8)**

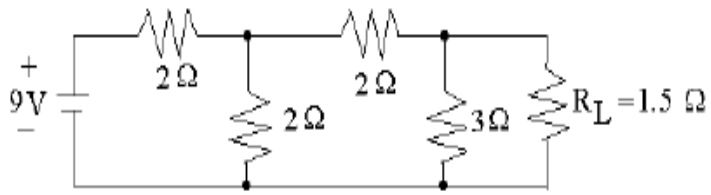

Fig.1

b. Explain Z parameters and also draw an equivalent circuit of the Z parameter model of the two port network. **(8)**

Q.3 a. An AC supply of 230V is applied to a half-wave rectifier circuit through transformer of turns ratio 5:1. Assume the diode is an ideal one. The load resistance is 300Ω. Find (a) dc output voltage (b) PIV (c) maximum value of power delivered to the load (d) average value of power delivered to the load. **(8)**

b. Define drift and diffusion current in PN junction diode. **(4)**

c. For PN diode, the reverse saturation current at a bias of 20V is 20nA. It is 5μA at 75 volts. Calculate DC resistances at these points**.** **(4)**

Q.4 a. Compare common emitter, common base and common collector configurations of amplifier. **(6)**

b. Explain the construction of Enhancement MOSFET with neat diagrams and also draw the output or drain characteristics. **(10)**

Q.5 a. Explain collector to base bias or collector feedback biasing method in detail and discuss the stability of the circuit. **(8)**

b. Draw the h parameters model of common emitter and derive the expression for current gain. **(8)**

Q.6 a. Draw & explain the Frequency response of amplifier and define 3 dB bandwidth. **(8)**

b. Derive the expression to calculate the higher cut-off frequency of the emitter follower amplifier. **(8)**

Q.7 a. The permissible range of a power transistor is defined $P(\max)=10W$, $I_c(\max)=1A, V_{CE}(\max)=100V, V_C(\min)=2V$

(i) Select an approximate operating point for operation in the circuit of Fig.2. Note that R_E has been considered to be negligible.

(ii) Specify R_L for maximum power output.

(iii) Calculate total dc power in, maximum signal power out, and overall efficiency. **(8)**

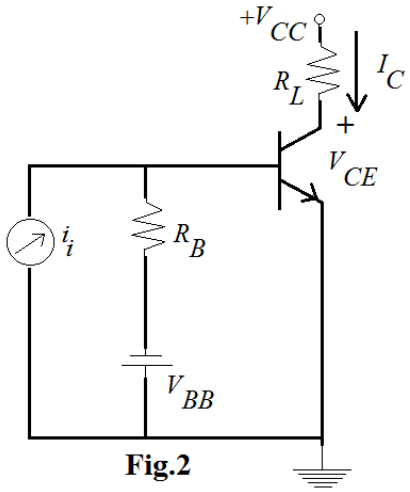

Fig.2

b. Show that the maximum efficiency of series fed class A power amplifier is 25%. **(8)**

Q.8 a. The voltage gain of an amplifier without feedback is 3000. Calculate the voltage gain of the amplifier if negative voltage feedback is introduced in the circuit. Given that feedback fraction = 0.01. **(4)**

b. Define negative feedback in amplifiers. **(4)**

c. Draw and explain Unijunction oscillator. **(8)**

Q.9 a. What do you mean by epitaxial growth in IC fabrication? Explain the steps involved in epitaxial growth. **(8)**

b. Explain the various steps involved in planar technology for device fabrication. **(8)**