ROLL NO. _____

Code: AC58/AT58/AC106/AT106 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT *{CURRENT & NEW SCHEME}*

Time: 3 Hours **DECEMBER 2015** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The full form of CPSR is
(A) Current Program Special Register
(B) Control Program Status Register
(C) Current Program Status Register
(D) Conditional Program Special Register

b. Return addresses in the case of subroutine nesting are used in
(A) LIFO **(B)** FIFO
(C) LILO **(D)** FILO

c. Memories that consist of circuits capable of retaining their state as long as power is applied are known as _____.
(A) Static Memory **(B)** Power Memory
(C) Dynamic Memory **(D)** Circuit Memory

d. 1M is equivalent to
(A) 2^{10} **(B)** 2^{20}
(C) 2^{15} **(D)** 2^{30}

e. When the I/O devices and the memory space share the same address space, the arrangement is called as _____.
(A) Memory-mapped I/O **(B)** Address controlled I/O
(C) Programmed memory I/O **(D)** Programmed I/O

f. Which is used to connect the processor to I/O devices that require transmission of data one bit at a time?
(A) Parallel port **(B)** Bridge
(C) Input-output interface **(D)** Serial port

g. The content of a 4-bit register is initially 1101. The register is shifted 2 times to the right with the serial input being 1011101. What is the content of the register after each shift?
(A) 1110, 0111 **(B)** 0001, 1000
(C) 1101, 1011 **(D)** 1001, 1001

h. The performance equation of a CPU is $T = \frac{N \times S}{R}$, where T is the processor time to execute a program; while N, S and R are respectively _____, ____ and _____.
(A) Number of instructions, Average number of steps and Number of Registers.
(B) Number of instructions, Average number of steps and Clock rate.
(C) Number of lines of a program, Size of program and Number of Registers.
(D) None of these.

i. CSA refers to
(A) Carry Sum Array **(B)** Carry Sum Addition
(C) Carry Save Adder **(D)** None of these

j. The registers, the ALU, and the interconnecting bus are collectively referred to as the _____.
(A) Datapath **(B)** Subpath
(C) Connecting path **(D)** None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. With the help of diagram, explain the different functional units of a Computer. **(6)**

b. Briefly explain about any four flags used by the processor to keep track of the information about the results of various operations. **(4)**

c. Explain the use of following registers:
(i) PC (ii) MAR
(iii) IR (iv) MDR **(1½ × 4)**

Q.3 a. Explain the following addressing modes with examples:
(i) Immediate mode
(ii) Relative mode
(iii) Auto increment **(2×3)**

b. Write a program that can evaluate the expression
X = (A-B) * ((C – D * E) / F)
in a single-accumulator processor. Assume that the processor has Load, Store, Multiply, Add instructions, and that all values fit in the accumulator. **(4)**

c. Write a program for adding a list of numbers implemented as a subroutine, LISTADD, with the parameters passed through processor registers. **(6)**

Q.4 a. Discuss handshaking scheme for controlling data transfers on the bus between the master and the slave. Explain the timing of an input data transfer using the handshake scheme. **(8)**

b. Define exception. Explain the different kinds of exceptions. **(8)**

Q.5 a. Draw the block diagram of serial interface and discuss the connection of processor to I/O devices using serial port. **(7)**

b. What are the sequences of events that take place when the processor sends a command to the SCSI controller? **(5)**

c. Explain how USB support Isochronous data. **(4)**

Q.6 a. Consider a memory consisting of 64K words of 8 bits each. Give the organization to implement this memory using 16K X 1 static memory chips. **(8)**

b. Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048 (2K) words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words, which we will view as 4K blocks of 16 words each. With the help of above given data, explain the following mapping techniques with proper diagram of cache and main memory:
(i) Associative Mapping
(ii) Set-Associative Mapping **(4×2)**

Q.7 a. With the help of suitable diagram, explain a circuit that can be used to perform either addition or subtraction of binary numbers. **(5)**

b. Define and draw the logic diagram of n-bit ripple-carry adder. **(6)**

c. Write short notes on DVD Technology. **(5)**

Q.8 a. Multiply the following pairs of signed 2's-complement numbers using:
(i) Booth algorithm (ii) Bit-pairing of the multiplier
A = 010111 and B = 110110
Assume A is the multiplicand and B is the multiplier. **(5+5)**

b. With the help of formats given by IEEE, explain IEEE standards for representing floating-point numbers. **(6)**

Q.9 a. Consider the statement ADD (R2), R1.
(i) Write the steps required for execution of above instruction.
(ii) Write the sequence of control steps required to perform the execution of above instruction for single bus architecture. **(6)**

b. With the help of block diagram, describe the complete processor. **(4)**

c. With the help of figure, explain multiple-bus organization. **(6)**