ROLL NO. _____

Code: DE58/DC58/DE108/DC108 **Subject: LOGIC DESIGN**

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **DECEMBER 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The binary equivalent of $(85.63)_{10}$ is
(A) 1010101.10100 **(B)** 1110101.10100
(C) 1010111.10100 **(D)** 1010101.11100

b. BCD code 01010011 represents decimal number _____.
(A) 52 **(B)** 53
(C) 256 **(D)** 51

c. A Karnaugh map with 4 variables has _____.
(A) 2 cells **(B)** 4 cells
(C) 8 cells **(D)** 16 cells

d. A memory that requires refreshing is _____.
(A) ROM **(B)** SRAM
(C) DRAM **(D)** Flash RAM

e. The sum of product of (A + B'C)(B + C'A) is_____.
(A) AB + AC' **(B)** AC + BC
(C) AB + AC **(D)** AC + B'C

f. In a 7 segment display, LEDs a, b and c light up. The decimal number displayed is _____.
(A) 9 **(B)** 7
(C) 1 **(D)** 3

g. A multiplexer having 32 data input lines needs _____ select lines.
(A) 5 **(B)** 3
(C) 4 **(D)** 8

h. In general the number of states = _____, where n is equal to the number of flip-flops.
(A) $1/2^n$ **(B)** 2^n
(C) 2n **(D)** n^2

i. A 4 bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each flip –flop is 100 nsec, the maximum clock frequency that can be used is equal to_____.
(A) 2.5 MHz **(B)** 5 MHz
(C) 25 MHz **(D)** 10 MHz

j. An 8 bit data is to be entered into a parallel in register. The number of clock pulses required is

(A) 2 **(B)** 1
(C) 4 **(D)** 8

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is a Digital System? Explain the advantages and limitations of Digital Techniques over Analog Techniques. **(8)**

b. Perform the following conversions. **(8)**
(i) $(111101.011)_2 = (\ )_{10}$ (ii) $(5267)_8 = (\ )_{10}$
(iii) $(68B)_{16} = (\ )_8$ (iv) $(1A2.C) = (\ )_{10}$

Q.3 a. Show, that how NAND and NOR gates are universal gates? **(8)**

b. Obtain (i) minimal sum of product (ii) minimal product of sum expression for function $F(A, B, C, D) = \Sigma (0, 2, 3, 6, 7, 8, 10, 11, 12, 15)$. **(8)**

Q.4 a. Draw and explain the operation of JK Flip Flop with the help of logic diagram. Also draw its truth table and timing diagram. **(8)**

b. Explain the application of Flip-Flop as a Shift Register using D Flip-Flops. **(8)**

Q.5 a. Build a Full Adder using two Half Adders and prove that the addition of two numbers results in subtraction when 2's complement is used. **(8)**

b. Perform followings using 2's complement method. **(4)**
(i) $(01001)_2 - (10100)_2$
(ii) $(100101)_2 - (100100)_2$

c. Draw the circuit diagram of 8 bit parallel adder. **(4)**

Q.6 a. What is a Ripple Counter? Draw the logic diagram of 3-bit Ripple Counter and explain its working with the help of timing diagram. **(8)**

b. Design 4 bit up/down binary ripple counter. **(8)**

Q.7 a. Design a BCD to excess 3 code converter using minimum number of NAND gates. **(8)**

b. Design a seven segment decoder that is required to drive an active low seven segment display. **(8)**

Q.8 a. Design a mod 7 synchronous counter and calculate its maximum frequency of operation if the flip flop delay time is 8 nano sec and gate delay time is 5 nano sec. **(8)**

b. Design 4 bit (serial In/Parallel out shift register), write the truth table with relevant diagram after 5 clock pulses. **(8)**

Q.9 a. How will you read and write into a 16×4 RAM? Draw a schematic of this RAM and explain the process. **(8)**

b. Design a combinational circuit using a ROM that accepts a 3-bit number and generates an output binary number equal to the square of the input number. **(8)**