ROLL NO. _____

Code: DE56/DE106 **Subject: ANALOG ELECTRONICS**

DipIETE – ET (Current & New Scheme)

Time: 3 Hours **DECEMBER 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Q2 to Q8 CAN BE ATTEMPTED BY BOTH CURRENT AND NEW SCHEME STUDENTS.**
- **Q9 HAS BEEN GIVEN INTERNAL OPTIOS FOR CURRENT SCHEME (DE56) AND NEW SCHEME (DE106) STUDENTS.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The Voltage gain of an Inverting Amplifier using OP-AMP is

(A) $1-\frac{R_f}{R_1}$ **(B)** $\frac{R_f}{R_1}$

(C) $1+\frac{R_f}{R_1}$ **(D)** $-\frac{R_f}{R_1}$

b. First layer in an IC is made up of _____.

(A) n-type material **(B)** P-type silicon substrate

(C) Thin SiO_2 layer **(D)** An aluminium layer

c. Which of the following BJT configuration has highest input resistance?

(A) CB **(B)** CE

(C) CC **(D)** CE-CC

d. The maximum collector efficiency of transformer coupled Class-A power amplifier is

(A) 50% **(B)** 78.5%

(C) 25% **(D)** 90%

e. What does the discharge transistor do in the IC 555 timer circuit?

(A) Charges the external capacitor to stop the timing

(B) Discharges the external capacitor to start the timing over again

(C) Discharges the external capacitor to stop the timing

(D) Charges the external capacitor to start the timing over again

f. The typical value of forward voltage drop across an LED is

(A) 0.7V **(B)** 1.0 V

(C) 0.3 V **(D)** 1.6 V

g. The maximum theoretical efficiency of a class B push-pull transistor power amplifier is approximately
(A) 25% **(B)** 50%
(C) 78.5% **(D)** 70.7%

h. With Zero volts on both inputs, an OPAMP ideally should have an output equal to
(A) zero voltage **(B)** negative supply voltage
(C) positive supply voltage **(D)** infinite voltage

i. The ideal value of slew rate for an op-amp is
(A) Zero **(B)** Infinite
(C) Low **(D)** Medium

j. The fastest Analog to Digital Converter technique is
(A) Parallel Comparator **(B)** Successive approximation
(C) Dual Slope **(D)** Counting type

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain Complementary MOSFET fabrication process with neat sketch. **(8)**

b. Explain any one of Basic Planar Processes used in IC fabrication. **(8)**

Q.3 a. In an NPN silicon transistor, the emitter-to-Collector Current gain (α) is 0.995, emitter current (I_E) = 10mA and leakage current (I_{CBO}) = 0.5 µA. Determine:
(i) Collector Current (I_C) (ii) Base Current (I_B)
(iii) Base-to-Collector Current Gain (β) (iv) I_{CEO} **(8)**

b. Explain the need for coupling and bypass capacitors in transistor circuits and draw AC Equivalent circuit of CE amplifier. **(8)**

Q.4 a. Explain the operating principle of N-channel JFET with the help of a neat diagram. **(8)**

b. The constant current circuit shown in Fig.1 uses a JFET whose operation is described by the equation $I_D = I_{DSS}(1-V_{GS}/V_P)^2$, $I_{DSS} = 8$ mA and $V_p = 4$ V **(8)**

(i) Draw the equivalent circuit as an amplifier
(ii) Calculate the required value of R to give a current of 0.5 mA
(iii) If the FET drain- source resistance r_{ds} is equal to 50 KΩ at I_D =0.5 mA, determine the incremental resistance of the circuit for the value of R calculated in (ii)

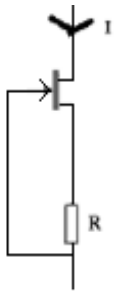

Fig.1

Q.5 a. With the help of a neat diagram, explain the working of Transformer coupled class B Push-Pull Power amplifier and show that its maximum collector efficiency is 78.6%. **(8)**

b. Describe the construction and working principle of Liquid Crystal Cell. **(8)**

Q.6 a. Discuss the characteristics of an ideal Operational Amplifier (Op-Amp). **(8)**

b. Discuss briefly the following terms with respect to Op-Amp: **(8)**
(i) Input bias current (ii) Input off-set voltage
(iii) Slew rate (iv) Power Supply Rejection Ratio (PSRR)

Q.7 a. Draw the circuit of inverting summing amplifier for 2 inputs using Op-Amp and drive an expression for its output voltage. **(8)**

b. Draw the circuit of an Instrumentation Amplifier using three Op-Amps and derive an expression for its output voltage. **(8)**

Q.8 a. Draw the circuit diagram of Triangular Waveform Generator using Op-Amp and describe its operation with waveforms. **(8)**

b. A 555 timer is configured to run in Astable mode with
R_A = 6.8 KΩ, R_B = 3.3KΩ and C = 0.1μF. Calculate
(i) T_{High} (ii) T_{Low}
(iii) Free running frequency (iv) Duty cycle (D) **(8)**

Q.9 (For Current Scheme student i.e. DE56)

a. What is meant by a voltage regulator? Explain series Op-Amp regulated power supply with the help of neat diagram. **(8)**

b. As shown in Fig. 2, if V_{in} = 20V, R = 200 Ω and V_z =12V, If V_{BE} = 0.65V, **(8)**
find
(i) Output Voltage (Vo)
(ii) The collector to emitter voltage of the pass transistor and
(iii) The current in the 200Ω resistor

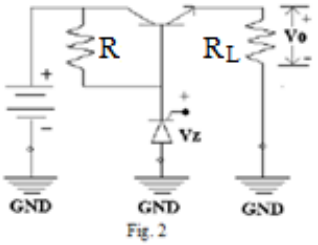

Fig. 2

Q.9 (For New Scheme student i.e. DE106)

a. What is meant by a voltage regulator? Explain series Op-Amp regulated power supply with the help of neat diagram. **(8)**

b. Explain the counter-type A/D converter with the help of suitable diagram and waveform. **(8)**