ROLL NO. _____

Code: DC57/DC107 **Subject: COMPUTER ORGANIZATION**

DipIETE – CS (Current & New Scheme)

Time: 3 Hours **DECEMBER 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. During the execution of the instruction, a copy of the instruction is placed in the
(A) Cache **(B)** RAM
(C) System heap **(D)** Register

b. The return address of the sub-routine is pointed by
(A) IR **(B)** PC
(C) MAR **(D)** Special memory register

c. When generating physical address from logical address the offset address is stored in
(A) Transaction look – aside buffer **(B)** Relocation register
(C) Shift Register **(D)** Page table

d. While using the iterative construct (branching) in execution. Which instruction is used to check the condition
(A) Test & Set **(B)** Branch
(C) Test condition **(D)** None of these

e. An optimizing compiler does
(A) Better combination of given piece of code
(B) Takes advantage of the type of processor and reduces it's process time
(C) Does better memory management
(D) Both **(A)** & **(C)**

f. Which method is used to map logical address of variable length onto physical memory?
(A) Paging **(B)** Overlays
(C) Segmentation **(D)** Paging with segmentation

g. A RAM chip has capacity of 1024 words of 8-bits each (1k X 8). The number of 2 X 4 with enable lines needed to construct a 16k X 16 RAM from 1k X 8 RAM is
(A) 4 **(B)** 6
(C) 5 **(D)** 7

h. DMA operation needs
(A) I/O bus
(B) a switch login between the I/O and system bus
(C) no processor control signal
(D) control signal such that DMA is after the processor accepts the hold request and sends hold acknowledgement

i. When a device interrupts, the processor finds the service routine address for processing from the
(A) Interrupt vector start address
(B) Processor program already under execution
(C) Interrupt vector location defined as per the device number
(D) Device control register

j. When 1101 is used to divide 100010010 the remainder is
(A) 101 **(B)** 11
(C) 0 **(D)** 1

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain different functional units of a digital computer. **(6)**

b. What is bus? Explain single bus structure architecture. Explain its advantage. **(5)**

c. What is Instruction and Instruction Sequencing? Explain Register Transfer Notation and Assembly Language Notation in brief. **(5)**

Q.3 a. What is an addressing mode? Explain different types of addressing mode. **(8)**

b. Explain with example, usage of stack in nested subroutine calls. **(8)**

Q.4 a. What is interrupt? What is interrupt service routine? Define hardware and software interrupt. **(8)**

b. Define different modes of Data transfer **(8)**
(i) Programmed I/O
(ii) Interrupt driven I/O
(iii) Direct memory Access

Q.5 a. Explain serial port and serial interface. **(8)**

b. What is USB? Explain USB architecture in detail. **(8)**

Q.6 a. Give comparison between SRAM & DRAM. **(8)**

b. Explain the secondary storage and explain working principle of magnetic disk. **(8)**

Q.7 a. Draw and explain virtual memory organization. **(8)**

b. Discuss direct mapped, associative mapped and set associative mapped cache memory system with suitable diagram. **(8)**

Q.8 a. Give Booth algorithm to multiply two binary numbers. Explain the working of algorithm taking an example. **(8)**

b. Explain IEEE standard floating point numbers. **(8)**

Q.9 a. Explain the hard wired control approach and micro-programmed control unit. **(8)**

b. Define the characteristics of RISC and CISC. **(8)**