ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **DECEMBER 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Channel resistance R_{ON} is scaled by
(A) $1/\alpha$ **(B)** $1/\beta$
(C) 1 **(D)** α/β

b. Scan path approach is implemented in
(A) LSSD **(B)** BST
(C) Both **(A)** and **(B)** **(D)** Logical Redundancy

c. What is Permittivity for free space?
(A) 5.85×10^{-14} Fcm^{-1} **(B)** 8.85×10^{-15} Fcm^{-1}
(C) 9.85×10^{-14} Fcm^{-1} **(D)** 8.85×10^{-14} Fcm^{-1}

d. What is the range for LSI?
(A) 10 **(B)** 100-1000
(C) 1000-20000 **(D)** 100000

e. Volatility is helpful in reduction of ……..
(A) Area **(B)** Data Storage Time
(C) Power dissipation **(D)** Scaling

f. Orange color in stick encoding scheme represents
(A) Polisilicon-2 **(B)** Polisilicon-1
(C) Via **(D)** V_{DD}

g. DRC at subsystem level is used to check
(A) Correct Wiring up of Leaf Cells **(B)** Correct Butting
(C) Both **(A)** and **(B)** **(D)** Correct mask making

h. Scanning E- beam Microscopes are disadvantageous due to
(A) Cost **(B)** Low resolution
(C) Slow **(D)** Less Reliable

i. Which model is suitable to represent a "stuck-at" fault?
(A) Mathematical model **(B)** Physical Model
(C) Logical Model **(D)** None of these

j. Which one is suitable for Testability?
(A) Controllability **(B)** Legibility
(C) Reliability **(D)** Availability

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Determine $Z_{P.U.}/Z_{P.D.}$ for an nMOS inverter driven by another nMOS inverter. **(6)**

b. Explain working of an nMOS transistor. Also derive expressions for g_m, g_{ds} and $\omega_{o.}$ **(10)**

Q.3 a. Describe n-well BiCMOS fabrication process steps. **(4)**

b. In an nMOS transistor operating at room temperature following measurements are done **(8)**
V_{GS}=4V V_{SB}=2.6V
V_{DS}=4V I_D=144μA
and the process parameters are
W/L=1, t_{ox}=400Å, $|2\Phi_F|$ = 0.64 V & $N_A=10^{16}/cm^3$
Find V_{th}, electron mobility and body effect coefficient. Assume oxide charge Q_{OX}=0

c. For an enhancement type MOS transistor the following parameters were measured. **(4)**
V_{T0} = 0.8V, $\gamma = 0.2V^{1/2}$, $|2\Phi_F|$=0.84V, K´=20μA/V^2, V_{GS}=2.8 V, V_{DS}=5V, V_{BS}= 0V &I_D=0.24mA. Find W/L.

Q.4 a. Discuss all possible pull-up alternatives for an nMOS inverter circuit. **(4)**

b. Explain lambda- based design rules for nMOS, pMOS and CMOS transistors. **(8)**

c. Discuss the concept of minimum sizes and overlaps in transistor design rules. **(4)**

Q.5 a. DiscussLatch-up problems and remedies in case of CMOS circuits. **(6)**

b. Discuss Parity generator circuit of a basic one-bit cell using stick diagrams. **(6)**

c. Explain, how super buffer circuits are helpful in delay reduction? **(4)**

Q.6 Describe the scaling effects in channel resistance, current density, power dissipation, substrate doping and substrate threshold currents. **(16)**

Q.7 a. Discuss Pseudo-nMOS, Dynamic and Clocked CMOS Logics in detail. **(12)**

b. Discuss briefly the procedure of testing a sequential circuit. **(4)**

Q.8 a. Explain optimization technique(s) of a Carry skip adder. **(10)**

b. Discuss the design of a pseudo-static RAM cell. **(6)**

Q.9 a. Give a qualitative analysis on Optimization of nMOS and CMOS inverters. **(10)**

b. Discuss BILBO scheme used in Built-in-self -test. **(6)**