ROLL NO. _____

**Code: AE66/AC66/AT66/AE108/AC108/AT108**
**Subject: MICROPROCESSORS & MICROCONTROLLERS**

## AMIETE – ET/CS/IT (Current & New Scheme)

**Time: 3 Hours** **DECEMBER 2018** **Max. Marks: 100**

***PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.***

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

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**Q.1 Choose the correct or the best alternative in the following: (2×10)**

**a.** 8085 µp is a _____ bit processor and it is decided by the _____.
**(A)** 16; internal data bus **(B)** 8; internal data bus
**(C)** 16; address bus **(D)** 8; address bus

**b.** Which of the following instruction is an example of implied addressing mode?
**(A)** MVI B, 99H **(B)** LHLD 2400H
**(C)** CMA **(D)** LDAX B

**c.** If the memory chip size is 1024 x 4 bits, how many chips are required to make up 2K memory?
**(A)** 4 **(B)** 2
**(C)** 6 **(D)** 8

**d.** Which of the following statement is not true for the instruction CMP B?
**(A)** Contents of Register B is subtracted from Register A.
**(B)** Contents of Flag Register is altered.
**(C)** Contents of Accumulator is altered.
**(D)** Contents of Accumulator is not altered.

**e.** ALE pin of 8085 µp goes high during _____ state and is used for _____ of the lower order address/data bus.
**(A)** T4; decoding **(B)** T1; de-multiplexing
**(C)** T2; multiplexing **(D)** T2; de-multiplexing

**f.** Which of the following statement is incorrect for I/O mapped I/O when compared to Memory mapped I/O?
**(A)** Maximum 256 I/O devices are possible in I/O mapped I/O while maximum 65535 devices are possible in Memory mapped I/O.
**(B)** I/O mapped I/O is slower as compared Memory mapped I/O.
**(C)** Complexity of the hardware for address decoding in I/O mapped I/O is less as compared to Memory mapped I/O.
**(D)** I/O mapped I/O uses an 8-bit address while Memory mapped I/O uses 16-bit address.

**g.** Which of the following pins of 8085 µp carry only data?
**(A)** $AD_0$-$AD_7$ **(B)** $AD_8$-$AD_{15}$
**(C)** SID & SOD **(D)** $S_0$ & $S_1$

**h.** Which of the following interrupt is not vectored?
**(A)** TRAP **(B)** INTR
**(C)** RST 7.5 **(D)** RST 0

**i.** What will be the status of all the ports of an 8255 PPI following a reset?
**(A)** All the ports will be in input mode.
**(B)** All the ports will be in output mode.
**(C)** All the ports will be tri-stated.
**(D)** There will be no change in port status.

**j.** In 8051 µp, to put the entire interrupt service routine in the interrupt vector table, it must be no more than _____ in size.
**(A)** 8 bytes **(B)** 4 bytes
**(C)** 16 bytes **(D)** 32 bytes

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks**

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**Q.2** a. Explain the stack operation while executing the following instructions assuming the stack pointer is initialised to 07FFH
(i) PUSH PSW, (ii) XTHL. **(4)**

b. Show with the help of a diagram, how the address and data lines are de-multiplexed. **(6)**

c. Write down the pins of 8085 with their brief description, to perform the following
(i) to reset the µp (ii) to reset the peripherals connected to the µp
(iii) to show the current status of the µp (iv) to provide the clock to the processor
(v) pins used in DMA transfer **(6)**

**Q.3** a. Why TMP register is connected in bidirectional with internal data bus of 8085 µp? **(4)**

b. Interface following with the 8085 using decoder in your design
(i) 2K x 8 ROM chip 1 No. (Starting address 0000H)
(ii) 256 x 8 RAM Chip 2 Nos. (Starting address 2000H) **(6)**

c. Differentiate among fetch, execute, machine and instruction cycle of an instruction with the help of a suitable example. **(6)**

**Q.4** a. Write an 8085 µp based program to clear all the flags of 8085 without affecting the contents of accumulator. **(4)**

b. In 8085 µp, the instructions INX and DCX do not affect any flag. What are the advantages and disadvantages of the same**?** **(6)**

c. Write an 8085 µp based program to convert 12 BCD numbers residing in locations starting from "NUMBER" to 12 binary numbers and store them in locations starting from "RESULT". **(6)**

**Q.5** a. Differentiate between Programmed I/O and Interrupt driven I/O. Mention the relative advantage of the second configurations of the same. **(4)**

b. Why an EI instruction is always written before the RET command of an Interrupt Service Routine (ISR)? Explain the two purposes for which SIM instruction is used. **(4)**

c. Write down the four different ways of disabling any interrupt. **(4)**

d. Differentiate among Port A, Port B and Port C of 8255 PPI. Write down the different modes of operation of 8255 PPI. **(4)**

**Q.6** a. Write an 8085 µp based assembly language program to display and blink "HELP US" using 8279 Keyboard and Display Controller. Assume the delay subroutine is available at 03E8H. **(8)**

b. Write an 8085 µp based assembly language program to input 256 bytes of data from a keyboard connected to Port A of 8255 PPI in mode 1 and output them to a parallel printer connected to Port B of 8255 PPI in mode 1. Use interrupt driven I/O for inputting and status check I/O for outputting. Assume inputting is always faster than outputting. **(8)**

**Q.7** a. Draw the block diagram of 8259 programmable interrupt controller and explain different modes of operation. How can it be expanded to handle 64 interrupt levels? **(8)**

b. Differentiate between Active and Idle cycles of 8237 DMA controller. Why DMA transfer is faster and how does it improve system performance? **(8)**

**Q.8** a. What is the advantage of Programmable Interval Timer (PIT)/ Counter over software designed timer/ counter? Draw the status of Clock, Gate and Out signals in mode 0 of 8253 PIT for a count value of five. **(8)**

b. Differentiate between the following in context of 8251A **(8)**
   i) Mode words and command words
   ii) Synchronous and Asynchronous Communication

**Q.9** a. Explain the operation of overflow flag of 8051 by giving suitable example. **(4)**

b. Draw the internal architecture of 8051 µc and discuss its features. **(6)**

c. Differentiate between General Purpose RAM (GPR) and Special Function RAM (SFR). Explain the memory organization of internal 128 bytes RAM**.** **(6)**