ROLL NO. _____

Code: AC58/AT58/AC106/AT106 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT (Current & New Scheme)

Time: 3 Hours **DECEMBER 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The central processing unit consists of
(A) ALU and MU **(B)** CU and MU
(C) ALU and CU **(D)** ALU and OU

b. The symbolic name of assembly language codes are also called as
(A) Binary language **(B)** Mnemonics
(C) High level language **(D)** Low level language

c. ISR stands for
(A) Interrupt Service Routine **(B)** Interrupt Service Subroutine
(C) Interrupt Subservice Routine **(D)** Interrupt Subservice Subroutine

d. The small extremely fast memory is called as
(A) Primary memory **(B)** Cache memory
(C) Secondary memory **(D)** External memory

e. Which memory is generally used to increase the apparent size of physical memory
(A) Secondary memory **(B)** Virtual memory
(C) Cache memory **(D)** Primary memory

f. The processor keeps track of the results of its operation using a flag called
(A) Conditional flag **(B)** Test flag
(C) Type flag **(D)** Zero flag

g. An interrupt that can be temporarily ignored is
(A) Vectored interrupt **(B)** Non-maskable interrupt
(C) Maskable interrupt **(D)** Low priority interrupt

h. The binary address issued to data or instruction is called as
(A) Physical address **(B)** Location address
(**C)** Relocatable address **(D)** Logical address

i. To convert virtual address into physical address, the programs are divided into
(A) Pages **(B)** Frames
(C) Segments (**D)** Blocks

j. Individual control words of the micro routine are called as

(A) Micro task **(B)** Micro operation

(C) Micro instruction **(D)** Micro commands

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Write the sequential steps of the operation of a computer. **(4)**

b. Draw and explain the connection between the processor and the memory unit. **(8)**

c. Explain the following address instruction **(4)**

ADD A, B

Mention clearly where the result is stored

Q.3 a. Explain the insertion and deletion operation of stack and queue structure with proper diagram. **(8)**

b. Briefly discuss subroutine and looping with proper example. **(8)**

Q.4 a. What is DMA? Explain how a 2-channel DMA controller works for 2 I/O devices, a disk drive and a high-speed printer. **(8)**

b. List the sequence of events in handling an INTR from a single device. **(6)**

c. Write short notes on INTR and INTA. **(2)**

Q.5 a. Explain with a neat block diagram, how a printer is connected to processor? **(8)**

b. Write the sequence of events that take place in the message exchange over SCSI bus. **(8)**

Q.6 a. Mention the priority with respect to size, speed and cost of cache memory, main memory and secondary memory. **(8)**

b. Explain LRU replacement algorithm in detail**.** **(8)**

Q.7 a. Represent the decimal values of 26, -37, 497 and -123 as signed 10-bit number in the following binary format. **(8)**

(i) 1's complement

(ii) 2's complement

b. Explain the address translation of virtual address to physical address in main memory with the help of page table. **(8)**

Q.8 a. Multiply 14 and -5 by using booth multiplication algorithm. **(8)**

b. Divide 1000 by 11 using restoring address, division algorithm. **(8)**

Q.9 a. Draw and explain the single-bus organization of the data paths inside the CPU. **(8)**

b. Elaborate the basic organization of a microprogrammed control unit with proper diagram. **(8)**