ROLL NO. _____

Code: AC103/AT103 Subject: ANALOG & DIGITAL ELECTRONICS

AMIETE – CS/IT *{NEW SCHEME}*

Time: 3 Hours **DECEMBER 2018** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part, each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. If an intrinsic semiconductor is doped with a very small amount of boron, then in the extrinsic semiconductor so formed, the number of electrons and hole will

(A) Decrease **(B)** Increase and decrease respectively
(C) Increase **(D)** Decrease and increase respectively

b. The junction capacitance of a linearly graded junction varies with the applied reverse bias, V_R as

(A) V_R^{-1} (B) $V_R^{-1/2}$
(C) $V_R^{-1/3}$ (D) $V_R^{1/2}$

c. In a rectifier, larger the value of shunt capacitor filter

(A) Larger the p-p value of ripple voltage
(B) Larger the peak current in the rectifying diode
(C) Longer the time that current pulse flows through the diode
(D) Smaller the DC voltage across the load

d. The following relationships between α and β are correct, except

(A) $\beta = \frac{\alpha}{1-\alpha}$ (B) $\alpha = \frac{\beta}{1-\beta}$
(C) $\alpha = \frac{\beta}{1+\beta}$ (D) $1-\alpha = \frac{1}{1+\beta}$

e. To avoid thermal runaway in the design of an analog circuit, the operating point of the BJT should be such that it satisfies the condition

(A) $V_{CE} = \frac{V_{CC}}{2}$ (B) $V_{CE} < \frac{V_{CC}}{2}$
(C) $V_{CE} > \frac{V_{CC}}{2}$ (D) $V_{CE} < 0.78V_{CC}$

f. While discussing amplifier performance, noise is defined as any kind of unwanted signal in the output which is

(A) Unrelated to the input signal **(B)** Derived from input signal
(C) Not generated by the amplifier **(D)** Due to associated circuitry

g. In binary numbers, by shifting the binary point one place to the right, the number

(A) Multiplies by 2 **(B)** Divides by 2
(C) Decreases by 10 **(D)** Increases by 10

h. Which gate represents the digital equivalent of an electric series circuit?

(A) NOR **(B)** NAND
(C) OR **(D)** AND

i. The dual of the statement (A+1) =1 is

(A) *A*.1=*A* **(B)** *A*.0 =0
(C) *A*+*A* =*A* **(D)** *A*.*A* =1

j. A 1 msec pulse can be converted to a 10 msec pulse by using

(A) An astable multivibrator **(B)** A monostable multivibrator
(C) A bistable multivibrator **(D)** A J-K flip-flop

PART A

Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. Describe the process of formation of bands in solids. Also define conduction band, valence band and forbidden energy gap outlining significance of each one of them. **(4)**

b. A block of silicon is doped with a donor atom density of $N_D = 3 \times 10^{14}$ atoms/cm^3, and with an acceptor atom density of $N_A = 0.5 \times 10^{14}$ atoms/cm^3. Determine the resultant densities of free electrons and holes. **(3)**

c. A bias is applied to a pn-junction, positive to the p-side and negative to the n-side. Show, by a series of sketches, the effect of this bias on depletion region width, Barrier voltage, minority carriers, and majority carriers. Briefly explain the effect in Each case. **(5)**

d. Sketch the complete equivalent circuits for forward biased and reverse biased diodes. Sketch the ac equivalent circuit for a forward biased diode. Briefly explain each circuit. **(4)**

Q.3 a. Draw the circuit diagram for a bridge rectifier, together with its input and output waveforms. Carefully explain the operation of the bridge rectifier circuit identifying the forward biased and reverse biased diodes during each half cycle of the input waveform. **(5)**

b. Draw the circuit diagram for a four stage voltage mltiplier circuit. Briefly explain its operation and identify the output terminals and the output voltage level relative to the input. Show how two additional diode capacitor circuits may be added and estimate the new output to input voltage ratio. **(6)**

c. A ±12 V square wave is applied to a circuit that cannot accept inputs in excess of ±4 V. The circuit input current is ±100 μ A. Design a suitable biased shut clipping circuit. **(5)**

Q.4 a. Sketch typical BJT common emitter current gain characteristics. Explain the shape of the characteristics. **(5)**

b. The base bias circuit shown in Fig.1 has R_B = 470 kΩ, R_C = 2.2 kΩ and V_{CC} = 18 V, and the transistor has h_{fe} = 100. Determine I_B, I_C and V_{CE}. **(6)**

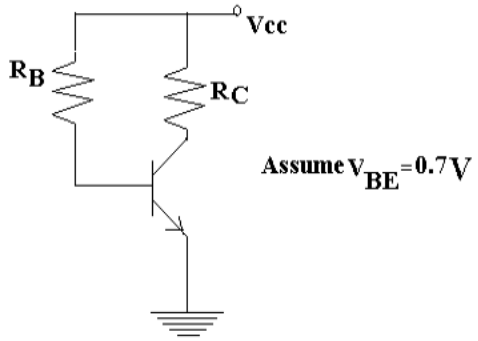

Fig.1

c. Show how a voltage-divider bias circuit may be compensated for V_{BE} changes with temperature. Derive an equation for I_C **(5)**

Q.5 a. Sketch a typical frequency response graph for an amplifier, and identify the upper And lower cut-off frequencies and the bandwidth. Briefly explain. **(5)**

b. Explain how phase shift distortion occurs in an amplifier, and discuss how negative feedback affects phase shift. **(5)**

c. Calculate the oscillating frequency for the Hartley oscillator shown in Fig. 2. If the components are R_1 = 3.3 *k*Ω, R_2 =56 *k*Ω,R_3 = 3.3 *k*Ω, L_1 = 3mH, L_2 = 50 mH and C_1 =1500 pF. **(6)**

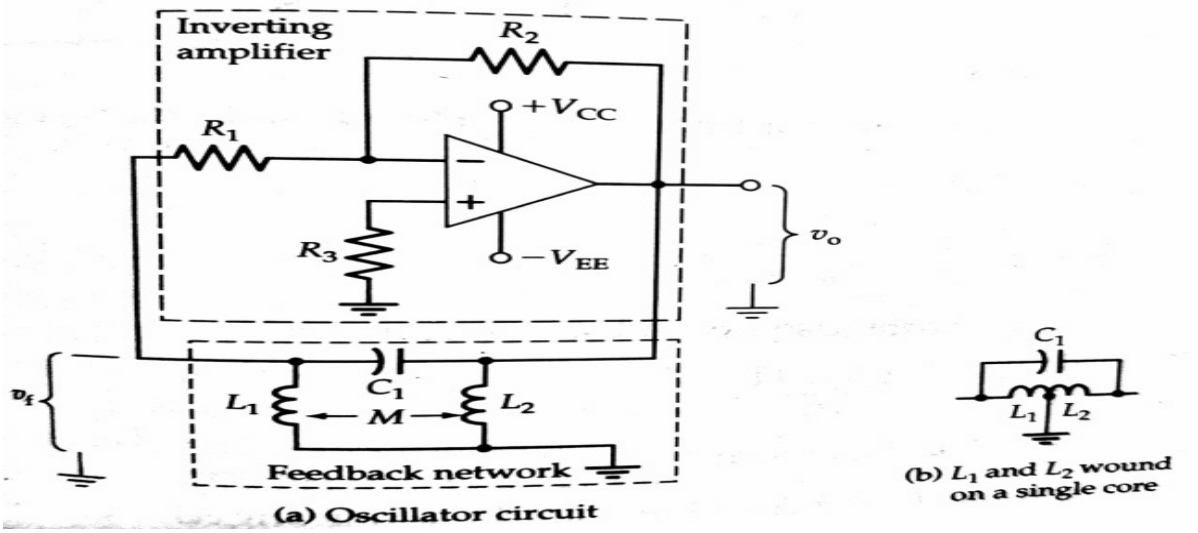

Fig. 2

PART B

Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Compare analog and digital systems highlighting relative merits and demerits. **(5)**

b. Convert 2313_{10} to octal and then to binary. **(3)**

c. Represent the statement " *X* = 25 / *Y* " in ASCII code **(3)**

d. Perform the following conversions **(5)**

(A) $1110101000100111_2 = (\ )_{10}$ (B) $511_{10} = (\ )_8$

(C) $3E1C_{16} = (\ )_{10}$ (D) $865_{10} = (\text{BCD})$

(E) $111010_2 = (\text{BCD})$

Q.7 a. State and prove De Morgan's theorem. **(8)**

b. Simplify the following expression using K-map

$y = \overline{(C+D)} + \bar{A}C\bar{D} + A\bar{B}\bar{C} + \bar{A}\bar{B}CD + AC\bar{D}$ using K-map **(8)**

Q.8 a. What is the range of unsigned decimal values that can be represented in 10 bits? What is the range of signed decimal values using the same number of bits. Also show the calculations involved. **(5)**

b. Design a look ahead carry circuit for the adder shown in Fig. 3 which generates the carry C_3 to be fed to the FA of the MSB position based on values of A_0 , B_0 ,C_0 , A_1, B_1, A_2 and B_2 . **(6)**

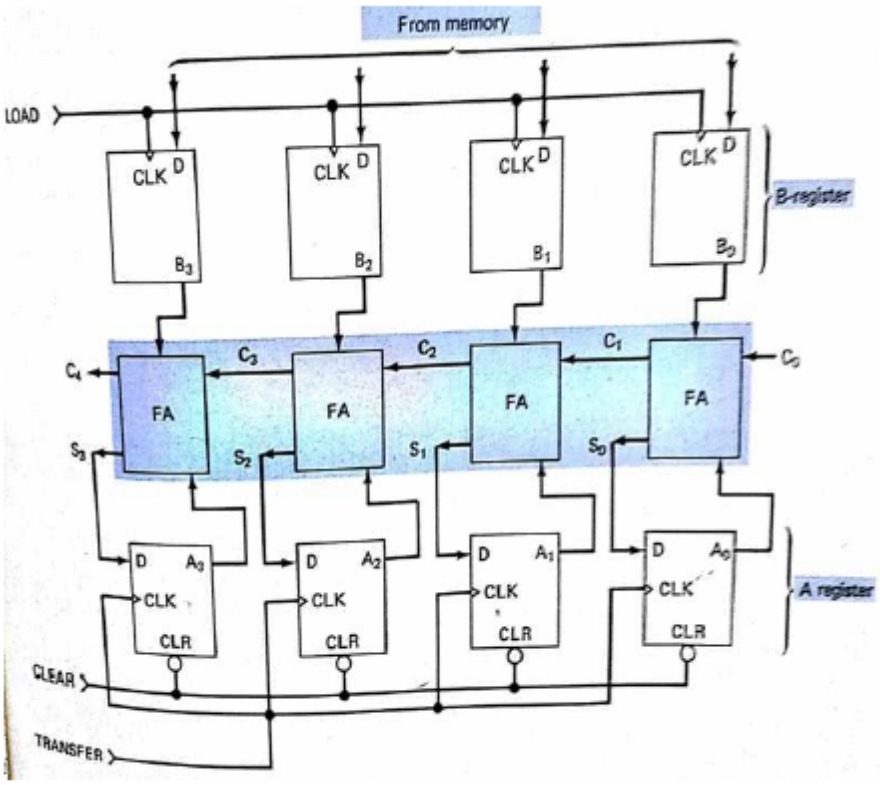

Fig 3.

c. Draw the schematic and explain the operation of a standard MSI encoder and decoder chips. **(5)**

Q.9 a. Show how the JK FF can be operated as a toggle FF. Apply a 10 kHz wave to its input and determine its output waveform. **(8)**

b. A 4-bit ripple counter is driven by a 20 MHz clock signal. Draw the waveforms at the output of each FF if each FF has $t_{pd} = 20\ ns$. Determine which counter states, if any, will not occur because of the propagation delays. **(8)**