ROLL NO. _____

Code: DE58/DC58/DE108/DC108 **Subject: LOGIC DESIGN**

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **December 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The Gray code of $(10111011)_2$ is _____
(A) 10011010 **(B)** 10011011
(C) 01100111 **(D)** 11100110

b. The Hexadecimal number equivalent of $(1001\ 01011101)_2$ is_____
(A) $(95D)_{16}$ **(B)** $(94D)_{16}$
(C) $(95C)_{16}$ **(D)** $(95B)_{16}$

c. A+$\bar{A}$ B is same as _____
(A) B **(B)** A+B
(C) A.B **(D)** 1

d. In Karnaugh map, Looping Groups of Eight is also called as _____
(A) Pair **(B)** Octet
(C) Quad **(D)** Cell

e. In a RS NAND latch, when R=1 and S=1, then Q(t+1) will be _____
(A) 1
(B) 0
(C) 1 or 0 depending on the value Q(t)
(D) $\bar{Q}$(t)

f. The logical expression for SUM of the full adder is _____
(A) $A \oplus B \oplus C$ **(B)** $\overline{A+B+C}$
(C) $\overline{A \oplus B \oplus C}$ **(D)** $\overline{A.B.C}$

g. A decade counter has_____ no of states count
(A) 9 **(B)** 8
(C) 10 **(D)** 11

h. How many lines are required to address 4096x8 memory chip_____
(A) 9 **(B)** 12
(C) 10 **(D)** 8

i. An N- bit register requires _____ no of flip flops
(A) N-1 **(B)** 2^N
(C) N **(D)** 2^{N-1}

j. The size of BCD Decoder is_____
(A) 10x4 **(B)** 4x10
(C) 16x4 **(D)** 4x16

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What are the advantages and limitations of digital techniques? **(6)**

b. Convert the decimal number 104.25 to its equivalent binary number. **(4)**

c. Convert the following numbers first into Binary code and then into Gray Code
(i) $(FBC)_{16}$ (ii) $(743)_8$ **(3x2)**

Q.3 a. Minimize the logic function F(W, X, Y, Z) = Σ m(2,3,4,5,6,7) + d(8,14,15) using K-maps and implement it with NAND gates only **(10)**

b. By using boolean algebra, prove that [$A\bar{B}$ (C+BD) + $\overline{AB}$] C = $\overline{AB}$C **(6)**

Q.4 a. Draw and explain the operation of JK Flip Flop with the help of logic diagram. Also draw its truth table and timing diagram. **(8)**

b. How JK Flip Flop can be used as T-Flip Flop and D- Flip Flop? **(4)**

c. What is the difference between Latch and Flip Flop? **(4)**

Q.5 a. Explain in detail, how two half adders and an OR gate can be used to implement a Full Adder? **(9)**

b. What are the various ways of representing signed number? Explain with example. **(7)**

Q.6 a. Explain the operation of Decade Counter with the help of neat diagram. Also draw its timing diagram. **(10)**

b. Differentiate between Asynchronous Counter and Synchronous Counter. **(6)**

Q.7 a. Design 1x4 demultiplexer. **(6)**

b. What is a Decoder? Draw the truth table for 4x16-line Decoder and implement the logic diagram from the truth table. **(10)**

Q.8 a. Design MOD5 synchronous counter and draw its logical diagram. **(8)**

b. Draw and explain the logic diagram for 4-bit Serial In Parallel Out (SIPO) Shift Register. **(8)**

Q.9 a. Draw and explain the internal organization of 64x4 RAM in detail. **(10)**

b. Explain the operation of dynamic memory cell. **(6)**