ROLL NO. _____

Code: DC57/DC107 Subject: COMPUTER ORGANIZATION

DipIETE – CS (Current & New Scheme)

Time: 3 Hours **DECEMBER 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to

(A) the time it takes for the platter to make a full rotation
(B) the time it takes for the read-write head to move into position over the appropriate track
(C) the time it takes for the platter to rotate the correct sector under the head
(D) none of these

b. In signed-magnitude binary division, if the dividend is $(11100)_2$ and divisor is $(10011)_2$ then the result is

(A) $(00100)_2$ **(B)** $(10100)_2$
(C) $(11001)_2$ **(D)** $(01100)_2$

c. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be

(A) 11 bits **(B)** 21 bits
(C) 16 bits **(D)** 20 bits

d. What is the content of Stack Pointer (SP)?

(A) Address of the current instruction
(B) Address of the next instruction
(C) Address of the top element of the stack
(D) Size of the stack

e. The maximum addressing capacity of a microprocessor which uses 16 bit data bus & 32 bit address bus is

(A) 64 K **(B)** 4 GB
(C) Both **(A)** & **(B)** **(D)** None of these

f. The gray code equivalent of $(1011)_2$ is

(A) 1101 **(B)** 1010
(C) 1110 **(D)** 1111

g. The cache memory of 1K words uses direct mapping with a block size of 4 words. How many blocks can the cache accommodate?

(A) 256 words **(B)** 512 words
(C) 1024 words **(D)** 128 words

h. The Cache memory works on the principle of

(A) Locality of data **(B)** Locality of memory
(C) Locality of reference **(D)** Locality of reference & memory

i. CPU does not perform the operation.....

(A) data transfer **(B)** logic operation
(C) arithmetic operation **(D)** all of these

j. $(2FAOC)_{16}$ is equivalent to …….

(A) $(195\ 084)_{10}$ **(B)** $(001011111010\ 0000\ 1100)_2$
(C) Both **(A)** and **(B)** **(D)** None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the various input output modes of data transfer. **(8)**

b. Differentiate between virtual and cache memory. **(8)**

Q.3 a. Discuss Flynn's classification of Computer. **(8)**

b. Differentiate between hardwired control and micro programmed control. **(8)**

Q.4 a. What is the difference between asynchronous and synchronous DRAM? **(8)**

b. Represent (-23) in:
(i) Sign-and-magnitude representation
(ii) 1's complement representation
(iii) 2's complement representation **(8)**

Q.5 a. Explain any four addressing modes giving suitable example. **(8)**

b. Explain the working of a microprogram sequencer with its block diagram. **(8)**

Q.6 a. Discuss the Arithmetic operations on floating point numbers. **(8)**

b. Explain Booth Algorithm for signed-operand multiplication. **(8)**

Q.7 a. Explain Universal Serial Bus Architecture. **(8)**

b. With the help of figure, explain multiple-bus organization, in detail. **(8)**

Q.8 a. Differentiate between the terms external, internal and software interrupts. **(8)**

b. A personal computer has main memory of 32K x 8 bytes and cache memory of 512 words. The cache is directly mapped with block size of 4 words.
(i) How many bits are required in tag, index block and word fields of the address format?
(ii) Show the addressing format.
(iii) What are the advantages of direct addressing scheme? **(8)**

Q.9 a. What do you mean by instructional pipeline? Explain its steps in detail. **(8)**

b. Draw the logic diagram of a 4 by 1 multiplexer with an enable input. **(8)**