ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **December 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Choose the fastest E-beam mask designing technique.
(A) Vector Scanning **(B)** Raster Scanning
(C) Both **(A)** & **(B)** **(D)** Raw Scanning

b. Which technology offers highest mobility?
(A) Bi-CMOS **(B)** CMOS
(C) NMOS **(D)** GaAs

c. Permittivity for afree space is given by
(A) 5.85×10^{-14} Fcm^{-1} **(B)** 8.85×10^{-14} Fcm^{-1}
(C) 9.85×10^{-14} Fcm^{-1} **(D)** 8.85×10^{-14} Fcm

d. Is it true that fast clock switching in digital VLSI circuits increase leakage power consumption as compared to static one?
(A) True **(B)** False
(C) Depends upon the application **(D)** None of these

e. The cost of memory _____ as access time is decreased
(A) Remains the same **(B)** Increases
(C) Decreases **(D)** May increase or decrease

f. For n inputs in a Wallace tree, growth of an adder cell is given by
(A) $\log_2(1/n)$ **(B)** $\log_2(n)$
(C) $\log_{10}(n)$ **(D)** None of these

g. Which device uses two metal layers in its stick encoding?
(A) nMOS **(B)** CMOS
(C) Both **(A)** & **(B)** **(D)** BiCMOS

h. Choose as a remedy for CMOS latch up problem from the following choices
(A) Decrease substrate doping level **(B)** Introduction of guard rings \
(C) Both **(A)** & **(B)** **(D)** Increasing contact resistance

i. BIST is helpful in
(A) Reduction in test time **(B)** Increasing test data volume
(C) Both **(A)** & **(B)** **(D)** None of these

j. RC delay _____ when line width becomes smaller.
(A) Increases **(B)** Decreases
(C) Both **(A)** & **(B)** **(D)** Can't Say

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

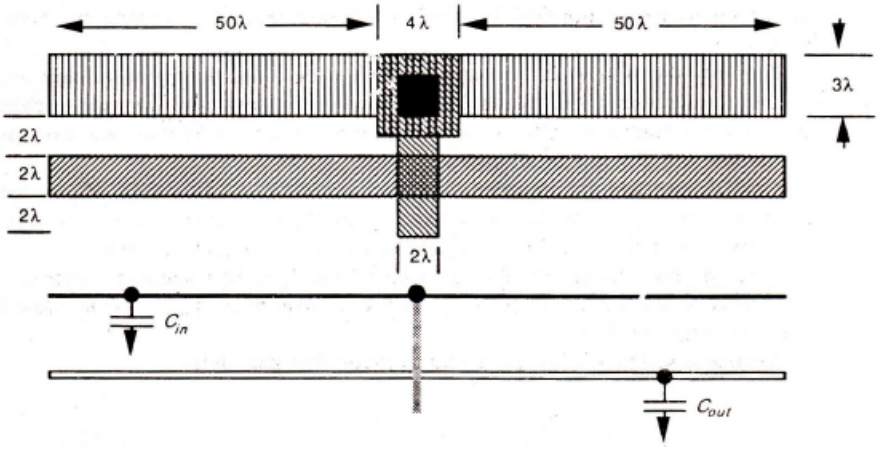
Q.2 a. Calculate $Z_{P.U.}/Z_{P.D.}$ for an nMOS inverter driven by another nMOS inverter. **(6)**

b. Describe working of an nMOS transistor. Also derive expressions for g_m, g_{ds} and ω_o. **(10)**

Q.3 a. Give Flow Diagram of Berkeley CMOS (n-well) fabrication technique. **(4)**

b. In an nMOS transistor operating at room temperature following measurements are done V_{GS}=4V V_{SB}=2.6V V_{DS}=4V I_D=144μA and the process parameters are W/L=1, t_{ox}=400Å, $|2\Phi_F|$ = 0.64 V&N_A=$10^{16}/cm^3$ Find V_{th}, electron mobility and body effect coefficient. Assume oxide charge Q_{OX}=0 **(8)**

c. Calculate C_{in} and C_{out} values of capacitances for the below given structure. **(4)**



Given

Capacitance	*Value in pF × $10^{-4}/\mu m^2$ (Relative values in brackets)*					
	5 μm		*2 μm*		*1.2 μm*	
Gate to channel	4	(1.0)	8	(1.0)	16	(1.0)
Diffusion (active)	1	(0.25)	1.75	(0.22)	3.75	(0.23)
Polysilicon* to substrate	0.4	(0.1)	0.6	(0.075)	0.6	(0.038)
Metal 1 to substrate	0.3	(0.075)	0.33	(0.04)	0.33	(0.02)
Metal 2 to substrate	0.2	(0.05)	0.17	(0.02)	0.17	(0.01)
Metal 2 to metal 1	0.4	(0.1)	0.5	(0.06)	0.5	(0.03)
Metal 2 to polysilicon	0.3	(0.075)	0.3	(0.038)	0.3	(0.018)

Notes: Relative value = specified value/gate to channel value for that technology.
*Poly. 1 and Poly. 2 are similar (also silicides where used).

Q.4 a. Discuss Lambda- based design rules for nMOS, pMOS and CMOS transistors. **(8)**

b. Draw Super Buffer and explain its advantages. **(8)**

Q.5 a. Explain the importance of Symbolic Diagram and give examples. **(8)**

b. Explain Inverter delays. **(8)**

Q.6 a. Discuss limitations of scaling in details. **(8)**

b. Draw the Bi-CMOS Structure of NAND Gate and explain. **(8)**

Q.7 a. Design a 4-bit Shifter and explain. **(8)**

b. Give a comparison of Adder Enhancement Technique. **(8)**

Q.8 a. Discuss the design of a pseudo-static RAM cell. **(8)**

b. Explain BIST. **(8)**

Q.9 a. Analyze qualitatively, the optimization techniques of nMOS and CMOS inverters. **(8)**

b. Explain the design flow of the CAD Tools. **(8)**