ROLL NO. _____

Code: AE68/AE117 **Subject: EMBEDDED SYSTEMS DESIGN**

AMIETE – ET (Current & New Scheme)

Time: 3 Hours **December 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Which characteristics of an embedded system exhibit the responsiveness to the assortments or variations in system's environment by computing specific results for real-time applications without any kind of postponement?
(A) Single-functioned characteristic
(B) Tightly-constraint Characteristics
(C) Reactive & Real time Characteristics
(D) All of these

b. Fetch instruction command means
(A) Reading instruction from keyboard to memory
(B) Reading instruction from memory into instruction register
(C) Reading instruction from instruction register to the decoder
(D) Fetching instruction from CPU to memory

c. The characteristics of an Harvard architecture are:
(A) Faster performance with separate Program and data memory.
(B) Faster performance with combined Program and data memory.
(C) Slow performance with combined Program and data memory.
(D) Slow performance with separate Program and data memory.

d. How many memory locations can a 16-bit PC can directly address?
(A) 65,536 **(B)** 60,000
(C) 1024 **(D)** 16

e. Select the wireless communication protocols
(A) CAN, IrDA and Bluetooth
(B) IrDA, Bluetooth and IEEE 802.11
(C) IEEE 802.11, I2C and FireWire
(D) FireWire, IEEE802.11 and CAN

f. The Processor relinquishes the buses during DMA control by activating the signals:
(A) DRQ and DACK **(B)** Int and INTA
(C) ACK and REQ **(D)** DRQ and ACK

g. Choose the right statements from the cache associative types
(A) In fully associative mapping compare all the addresses stored in the cache with the desired address.
(B) In set-Associative mapping simultaneously compare all the tags at that location with the desired tag.
(C) In direct mapping compare stored tag with the desired tag.
(D) All of these

h. Evaluate resolution of DAC for Vmax=5V,n=8.
(A) 256 **(B)** 0.0196
(C) 0.0392 **(D)** 255

i. The problem of priority inversion can be solved by
(A) priority inheritance protocol **(B)** priority inversion protocol
(C) Both **(A)** and **(B)** **(D)** None of these

j. The memory type showing best storage permanence is
(A) SRAM **(B)** OTP ROM
(C) EPROM **(D)** Mask Programmable ROM

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Define Embedded System and highlight its characteristics with example of a digital camera. **(9)**

b. Bring out comparison between the following: **(7)**
(i) Full custom Vs. Semi-Custom
(ii) Single purpose processor Vs. General Purpose processor

Q.3 a. Explain the techniques used for improving throughput of a microprocessor. **(4)**

b. Explain the software development process with a neat block diagram. **(6)**

c. With a neat block diagram explain architecture of a general purpose processor. **(6)**

Q.4 a. Explain the functionality of following peripheral devices of an embedded system: Timers, Counters and watch dog timers. **(6)**

b. With the help of hardware and software implementation, explain the controlling of a stepper motor. **(8)**

c. Draw neat waveform of a pulse width modulator showing 75% duty cycle. **(2)**

Q.5 a. Explain three types of cache mapping techniques with neat diagrams. **(10)**

b. Write brief note on SRAM, DRAM and NVRAM. **(6)**

Q.6 a. Explain and compare the following: **(6)**
(i) Standard I/O and Memory mapped I/O
(ii) Priority and daisy chain arbitration

b. List out the popular serial communication protocols and explain any one of them in detail. **(6)**

c. Briefly explain the steps of microprocessor interfacing techniques DMA. **(4)**

Q.7 a. Discuss methods to prevent shared-data problems. **(6)**

b. Define Semaphore. With the help of flowchart explain execution of tasks with semaphores. **(10)**

Q.8 a. Define message Queues, mailboxes and pipes. **(6)**

b. Define interrupt routines in RTOS. Explain with the help of timing diagram interrupt Service Routing flow for nested interrupts. **(10)**

Q.9 a. Explain design considerations of RTOS based embedded system. **(6)**

b. Explain power saving modes in an Embedded System. **(4)**

c. What is encapsulating? Explain any one type of encapsulating techniques used in RTOS. **(6)**