ROLL NO. _____

Code: AE54/AC54/AT54/AE104
Subject: LINEAR ICs & DIGITAL ELECTRONICS

AMIETE – ET/CS/IT (Current & New Scheme)

Time: 3 Hours **December 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions, selecting at least TWO questions from each part. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The slew rate of an ideal op-amp is
(A) very slow **(B)** slow
(C) fast **(D)** infinitely fast

b. The open loop gain of an ideal op-amp is
(A) infinite **(B)** very high
(C) neither high nor low **(D)** low

c. The output impedance of an ideal op-amp is
(A) zero **(B)** low
(C) high **(D)** infinite

d. The input impedance of an ideal op-amp is
(A) zero **(B)** low
(C) high **(D)** infinite

e. The bandwidth of an ideal op-amp is
(A) zero **(B)** low
(C) high **(D)** infinite

f. A mod 4 counter will count
(A) from 0 to 4 **(B)** from 0 to 3
(C) from any number n to n+4 **(D)** None of these

g. In a JK Flip Flop toggle means
(A) Set Q=1 and $\overline{Q}$=0 **(B)** Set Q=0 and $\overline{Q}$=1
(C) Change the output to opposite state **(D)** No change in output

h. The number of Inputs and Outputs in a full adder are
(A) 2 & 1 **(B)** 2 & 2
(C) 3 & 3 **(D)** 3 & 2

i. In a 4 input AND Gate , the total no. of High Outputs for 16 input states are
(A) 16 **(B)** 8
(C) 4 **(D)** 1

j. The number of bits in a nibble are
(A) 8 **(B)** 4
(C) 2 **(D)** 16

PART A
Answer at least TWO questions. Each question carries 16 marks.

Q.2 a. What is an op-amp? List four basic building blocks of an op-amp. **(4)**

b. Explain briefly the difference between digital and linear IC's. **(4)**

c. What is the difference between monolithic and hybrid IC's? **(4)**

d. What is the major difference among SSI, MSI, LSI and VLSI IC's? **(4)**

Q.3 a. Draw non-inverting amplifier using op-amp, with negative feedback. Derive an expression for its voltage gain and input impedance with feedback. **(12)**

b. An op-amp having the following parameters is connected as non-inverting amplifier with R_1 = 1 kΩ, R_F = 10 kΩ, A = 200000 & R_i = 2 MΩ. Calculate A_F and R_{iF} **(4)**

Q.4 a. Explain Schmitt Trigger with suitable circuit diagram, waveforms and equations. **(8)**

b. Draw and explain peak detector circuit along with suitable waveforms. **(8)**

Q.5 a. Draw and explain the working principle of astable multivibrator using IC555 along with suitable waveforms and equations. **(8)**

b. Explain the operation of successive approximation type analog to digital converter using suitable diagram. **(8)**

PART B
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Define bit, byte, nibble and word. **(8)**

b. (i) Covert $(25.5)_{10}$ to Binary
(ii) Convert $(0.10101)_2$ to Decimal
(iii) Convert $(1001110)_2$ to Octal
(iv) Convert $(10100110101111)_2$ to Hexadecimal **(8)**

Q.7 a. Minimize the following four variable logic function using K-Map and realize the minimized function using NAND Gates.
$f(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$ **(10)**

b. (i) Simplify the expression $\left(A + \overline{B} + \overline{C}\right)\left(A + \overline{B} + C\right)$
(ii) Prove that $ABC + D\overline{C} + ABD = ABC + D\overline{C}$ **(6)**

Q.8 a. Perform the following operations using 2's complement method.
(i) 48-23 (ii) 23-48
(iii) 48-(-23) (iv) -48-23.
Use 8-bit representation of numbers. **(8)**

b. Explain Comparator with proper block diagram and draw truth table for a 2-bit Comparator. **(8)**

Q.9 a. Draw logic circuit diagram of clocked S-R & J-K Flip Flops using NAND Gates along with their Truth Tables. **(8)**

b. Design a natural binary sequence mod-8 synchronous counter using D Flip flops. **(8)**