ROLL NO. _____

Code: AC58/AT58/AC106/AT106 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT (Current & New Scheme)

Time: 3 Hours **December 2016** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The full form of CPSR is
(A) Current Program Special Register
(B) Control Program Status Register
(C) Current Program Status Register
(D) Conditional Program Special Register

b. The content of a 4-bit register is initially 1101. The register is shifted 2 times to the right with the serial input being 1011101. What is the content of the register after each shift?
(A) 1110, 0111 **(B)** 0001, 1000
(C) 1101, 1011 **(D)** 1001, 1001

c. The control unit controls other units by generating
(A) Control signals **(B)** Timing signals
(C) Transfer signals **(D)** Command Signals

d. A two input NOR gate gives logic high output only when
(A) one input is high **(B)** one input is low
(C) Both inputs are low **(D)** Both inputs are high

e. Interrupts which are initiated by an instruction are
(A) internal **(B)** external
(C) hardware **(D)** software

f. In a program using subroutine call instruction, it is necessary to
(A) Initialise program counter **(B)** Clear the accumulator
(C) Reset the microprocessor **(D)** Clear the instruction register

g. When the I/O devices and the memory space share the same address space, the arrangement is called as _____.
(A) Memory-mapped I/O **(B)** Address controlled I/O
(C) Programmed memory I/O **(D)** Programmed I/O

h. How is data stored in the main memory?
(A) Bytes **(B)** Words
(C) Pages **(D)** Both **(A)** and **(B)**

i. 4 bit CLA addition process requires
(A) 4 gate delay **(B)** 3 gate delay
(C) 1 XOR gate delay **(D)** 2 gate delay

j. The number 100110_2 is numerically equivalent to
(A) 26_{10} **(B)** 36_{10}
(C) 46_8 **(D)** $2A2_{16}$

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What are the different performance measures used to represent a computer system's performance? **(6)**

b. Describe in brief the different generations of computer. **(4)**

c. Explain basic instruction types with the help of examples. **(6)**

Q.3 a. Write a program that can evaluate the expression
X = (A – B) * ((C – D * E) / F)
in a single-accumulator processor. Assume that the processor has Load, Store, Multiply, Add instructions, and that all values fit in the accumulator. **(4)**

b. Explain how stack is used for nested subroutines. Show the flow of execution using a suitable example. **(8)**

c. Explain the following addressing modes with examples: **(2×2)**
(i) Immediate mode
(ii) Relative mode

Q.4 a. When a DMA module takes control of bus and while it retains control of bus, what does the processor do? **(6)**

b. Describe the three types of Input / Output techniques, viz., Programmed Input /Output Interrupt driven Input / Output and Direct Memory Access. **(10)**

Q.5 a. Describe the main phases involved in the operation of the SCSI bus. **(8)**

b. Describe the Peripheral Component Interconnect (PCI) Bus Standards. **(4)**

c. Explain how USB support Isochronous data? **(4)**

Q.6 a. Explain briefly SRAM and DRAM. Mention the differences between these. **(5)**

b. Why RAM traditionally has been organized as only one bit per chip where as ROM is organized with multiple chips per bit? **(5)**

c. Explain the cache with two-way set-associative addressing. Give an illustration. **(6)**

Q.7 a. Draw a flow chart to explain how addition and subtraction of two fixed point numbers can be done. Give an example to explain it. **(8)**

b. How virtual memory address translation is done? Explain with the help of a diagram. Compare cache techniques and virtual memory techniques. **(6+2)**

Q.8 a. Multiply the following pairs of signed 2's-complement numbers using:
(i) Booth algorithm (ii) Bit-pairing of the multiplier
A = 010111 and B = 110110
Assume A is the multiplicand and B is the multiplier. **(5+5)**

b. Discuss any two IEEE standard floating point formats. Explain Add/Subtract and multiply rules on floating point numbers. **(6)**

Q.9 a. With suitable figure, discuss multiple-bus organization. **(6)**

b. Distinguish between horizontal and vertical microinstruction. **(5)**

c. Write the actions required to execute the instructions Move(R1), R2. **(5)**