ROLL NO. _____

DipIETE – ET/CS (NEW SCHEME) – Code: DE67/DC67

Subject: EMBEDDED SYSTEMS

Time: 3 Hours **Max. Marks: 100**

DECEMBER 2011

NOTE: There are 9 Questions in all.

- **Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.**
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. A Sequential circuit is a digital circuit whose outputs are a function of

(A) Present as well as previous input values.
(B) Present values
(C) Previous values
(D) None of the above.

b. Complex state diagram is referred as

(A) FSMD **(B)** FSM
(C) FSD **(D)** FMD.

c. Which of the following is incorrect common design metrics

(A) Size, Performance, Flexibility
(B) Maintainability, Correctness, Safety
(C) NRE cost, unit cost, power
(D) Rigid, linearity, sturdy

d. Emulator supports

(A) Debugging of the program while it executes on development processor
(B) Debugging of the program while it executes on target processor
(C) Programmers to evaluate and correct their programs
(D) Programmers to convert HLL to MLL

e. Resolution of ADC is given by

(A) $\frac{V_{max}}{2^n - 1}$ **(B)** $\frac{V_{min}}{2^n - 1}$

(C) $\frac{V_{max}}{2^n}$ **(D)** $\frac{V_{min}}{2^n}$

f. PCI bus is used for

(A) Interconnecting chips
(B) Connecting expansion boards
(C) Connecting processor memory subsystem
(D) All the above

g. Which one is not cache replacement policy

(A) Random **(B)** Least recently used
(C) First in first out **(D)** Write through

h. Which one of the following is not a semaphore variant

(A) counting semaphore **(B)** resource semaphore
(C) mutex semaphore **(D)** dormant semaphore

i. Each task can be in one of the following three states

(A) Running, Ready , Blocked **(B)** Running, Interrupted, Ready
(C) Stopped, Blocked, Ready **(D)** None of the above

j. Events are one bit flags

(A) with which tasks signal one another
(B) with which tasks are executed
(C) with which tasks are terminated
(D) none of the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain design metrics used for embedded systems. **(10)**

b. Compute the annual growth rate of IC capacity and designer productivity **(6)**

Q.3 a. Explain the steps involved in sequential logic design right from state diagram to combinational logic diagram for the problem given below

Construct a pulse divider slow down your pre existing pulse so that you output a 1 for every four pulses detected **(12)**

b. Answer the following:
(i) What is the difference between synchronous and an Asynchronous circuits? **(2)**
(ii) Why NAND and NOR gates are more common than AND and OR gates? **(2)**

Q.4 a. Explain the following **(10)**
(i) Linker
(ii) Cross compiler
(iii) device programmers
(iv) Emulators
(v) Debuggers

b. With example explain how program and data memory can be overlapped in a Harvard architecture **(6)**

Q.5 a. Explain the functions of timers, reaction timers and watchdog timers **(9)**

b. Given a timer with a terminal count and a clock frequency of 10 Mhz, calculate the following **(7)**
(i) Range and resolution
(ii) Terminal count value needed to measure 3ms intervals
(iii) If a prescalar is added, what is the minimum division needed to measure an interval of 100ms
(iv) Instead of a prescalar a second 16 bit up-counter is cascaded, what is the range and resolution of this design

Q.6 a. Explain direct and fully associative cache mapping technique **(8)**

b. Sketch the internal design of 8X4 ROM and Explain? **(8)**

Q.7 a. Explain in brief serial protocols which are widely used? **(8)**

b. Explain how to extend the number of ports on a 4 port 8051 to 8 port by using extended parallel I/O. Draw and label all interconnection and I/O ports clearly indicating the names and widths of all connections. **(8)**

Q.8 a. Briefly explain the function of scheduler. **(8)**

b. Explain in brief any two methods or ways to protect shared data? **(8)**

Q.9 a. Explain ACVM hardware architecture with the help of a block diagram. **(8)**

b. Briefly explain Digital Camera Software Architecture. **(8)**