

DipIETE – ET/CS (NEW SCHEME) – Code: DE58 / DC58**Subject: LOGIC DESIGN**

Time: 3 Hours

DECEMBER 2011

Max. Marks: 100

NOTE: There are 9 Questions in all.

- Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.
- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Parity method is used to

- (A) correct an error (B) detect an error
(C) detect and correct an error (D) none of the above

b. According to Boolean theorem $(\bar{A} + B)(A + B) =$

- (A) B (B) A
(C) $\bar{A}B$ (D) AB

c. The synchronous inputs in JK flipflop are

- (A) J and K (B) clock and $\overline{\text{clock}}$
(C) Preset and clear (D) none of the above

d. The number 11010 is a signed binary number in 2's complement system, the decimal value of this number is

- (A) -8 (B) -6
(C) 26 (D) 10

e. If $t_{pd} = 12\text{ns}$ of a J-K flip flop, the largest MOD counter that can be constructed to operate upto 10 MHz is

- (A) MOD 8 (B) MOD 12
(C) MOD 4 (D) MOD 16

		CD			
		00	01	11	10
AB	00	1	1	1	1
	01	1	1	0	0
	11	0	0	0	1
	10	0	0	1	1

Fig.1

- Q.4** a. Explain Race around condition occurs in Flip-Flop. How it can be avoid or minimize it. (8)
- b. With neat internal circuitry of the negative edge triggered JK flip flops explain its operation. (8)
- Q.5** a. Perform followings using 2's complement method
 (i) $(01001)_2 - (10100)_2$ (ii) $(100101)_2 - (100100)_2$ (4)
- b. Design a full adder using decoder. (8)
- c. Draw the circuit diagram of 8 bit parallel adder. (4)
- Q.6** a. Design a synchronous counter using T-FF that counts from 0111 to 0010. (8)
- b. Design up/down 4 bit binary ripple counter. (8)
- Q.7** a. Compute the condition when De-MUX behave as a decoder. Realize full subtracter using De-Multiplexers. (8)
- b. Design 8:1 multiplexer using NAND gates. (8)
- Q.8** a. Design a 4 bit bi-directional shift register using DFF. (8)
- b. Design 4 bit (serial In/Parallel out shift register), write the truth table with relevant diagram after 5 clock pulses. (8)
- Q.9** a. With neat diagram explain RAM architecture. (8)
- b. Design a combinational circuit using a ROM that accepts a 3-bit number and generates an output binary number equal to the square of the input number. (8)