ROLL NO. _____

Code: AE74 Subject: VLSI DESIGN

AMIETE – ET (NEW SCHEME)

Time: 3 Hours **DECEMBER 2011** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.**
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Which of the following layer developed first during fabrication?

(A) Source **(B)** Drain
(C) Gate **(D)** Metal Contact

b. The Gate capacitance of a MOS Transistor is given by

(A) $\frac{\in_{ins}\in_o \mu}{D}$ **(B)** $\frac{\in_{ins}\in_o A}{V_{gs}}$

(C) $\frac{\in_{ins}\in_o A}{I_{ds}}$ **(D)** $\frac{\in_{ins}\in_o WL}{D}$

c. The Trans-conductance of a MOS device can be increased by increasing its

(A) Length **(B)** Threshold Voltage
(C) Width **(D)** Oxide thickness

d. Two NMOS pass transistors with V_t = 1.2V are connected in cascade such that drain of first is connected to source of the next and gate of both MOS are connected to 5V. The Output voltage V_o is

(A) 2.6V **(B)** 3.8V
(C) 1.2V **(D)** 0V

e. The sheet resistance of a square is _____ to its thickness.

(A) inversely proportional **(B)** directly proportional
(C) not related **(D)** equal

f. N-well CMOS fabrication process uses _____substrate.

(A) P-type Semiconductor **(B)** N-type Semiconductor
(C) Pure conductor **(D)** Pure Insulator

g. Super buffer is used to

(A) Increase asymmetry in rise and fall times
(B) Reduce asymmetry in rise and fall times
(C) Increase rise time and reduce fall time
(D) None of the above

h. The Switch logic is based on

(A) Pass transistors only
(B) Transmission gates only
(C) Pass transistors and transmission gates
(D) inverter circuits

i. The total number of transistors required to realize 2-input Bi-CMOS NAND gate including discharging path transistors are

(A) 4 MOS transistors and 2 BJTs **(B)** 3 MOS transistors and 2 BJTs
(C) 2 MOS transistors and 2 BJTs **(D)** 7 MOS transistors and 2 BJTs

j. In a three-transistor dynamic RAM cell, the data read output onto the bus is

(A) Same as stored bit **(B)** Complement of the stored bit
(C) 2's complement of the stored bit **(D)** One, irrespective of stored bit

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Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the action of N-MOS Enhancement mode transistor for different values of V_{gs} and V_{ds}. **(8)**

b. What are the advantages of E-beam masks? Differentiate between Raster scanning and Vector scanning. **(4)**

c. Draw the cross-sectional view of p-well CMOS inverter and indicate the input, output and supply voltages. **(4)**

Q.3 a. Calculate the threshold voltage with $\epsilon_{si}=11.7$, $\epsilon_{ox}=3.9$ for an N-MOS transistor with $N_A=2\times10^{17}/cm^3$, $t_{ox}=190\,\mathring{A}$. Assume $\Phi_{ms}=-0.85V$, $N_i=1.45\times10^{10}/cm^3$ and $Q_{fc}=Q_{ss}=V_{SB}=0$. **(8)**

b. Explain the CMOS inverter transfer characteristics by highlighting the regions of operation of the MOS transistor. **(8)**

Q.4 a. Discuss λ-based n-MOS design rules for wires and contacts. **(8)**

b. Describe the monochrome stick encoding of:

(i) Simple n-well based BiCMOS inverter
(ii) 2-input CMOS NAND gate. **(8)**

Q.5 a. Derive the expressions for rise time and fall time of CMOS inverter and show that $\tau_r = 2.5\ \tau_f$ for equal n and p-transistor geometries. **(8)**

b. Find the static on-state resistance of a 4:1 N-MOS inverter and minimum sized CMOS inverter. (Assume on resistance of minimum sized NMOS enhancement transistor as $10K\Omega$) **(6)**

c. Draw the circuit of non inverting type N-MOS super buffer. **(2)**

Q.6 a. Obtain the Scaling Factors for the following Device Parameters: **(8)**
(i) Switching energy per gate
(ii) current density
(iii) gate delay
(iv) gate capacitance

b. Realize 4:1 multiplexer using N-MOS switches. **(4)**

c. Show that for an 8:1 N-MOS inverter with minimum sized pull-down transistor, the on state power dissipation is 0.28 mw. (Power supply = 5V) **(4)**

Q.7 a. Discuss the linking of the subunits using one bus, two bus and three bus architectures with suitable diagrams. **(8)**

b. Design a single bit adder and implement 4-bit ALU functions using adder elements. **(8)**

Q.8 a. What are the system timing considerations? **(6)**

b. Explain with circuit diagram the functioning of a three-transistor dynamic RAM cell. What are the conditions for no power dissipation in the cell? **(6)**

c. What are noise margins? Write the CMOS inverter noise margin equations with the help of CMOS inverter transfer characteristics. **(4)**

Q.9 Write short notes on (Any **FOUR**): **(4×4)**

(i) CAD tools for VLSI design
(ii) Design for testability
(iii) Testing sequential logic
(iv) Built-In-Self-Test (BIST)
(v) Ground rules for successful design.