ROLL NO. _____

Code: AE09 Subject: ANALOG & DIGITAL ELECTRONICS

AMIETE – ET (OLD SCHEME)

Time: 3 Hours **DECEMBER 2011** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.**
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. The rate of change of an integrator's output voltage in response to a step input is set by

(A) The RC time constant
(B) The amplitude of the step input
(C) The current through the capacitor
(D) all of these

b. In a 4-bit binary weighted input DAC, if the lowest valued resistor is $1K\Omega$, the highest valued input resistor is

(A) $1\ K\Omega$ **(B)** $4\ K\Omega$
(C) $8\ K\Omega$ **(D)** $16\ K\Omega$

c. The type of ADC with the fastest conversion time is the

(A) Dual slope **(B)** Single slope
(C) Simultaneous **(D)** Successive approximation

d. The output of a particular op-amp increases 8V in 12μs. The slew rate is

(A) 96 V/μs **(B)** 0.67 V/μs
(C) 1.5 V/μs **(D)** None of these

e. The frequency at which the open loop gain is equal to one is called

(A) The upper critical frequency **(B)** Cutoff frequency
(C) The notch frequency **(D)** The unity gain frequency

f. In ECL negative supply voltage is used because of

(A) Reduction in noise at the output **(B)** Saving in power
(C) Case of wired-OR operation **(D)** Increase in speed of operation

g. The figure of merit of a logic family is given by

(A) Gain x bandwidth
(B) Propagation delay time x power dissipation
(C) Fan-out x propagation delay time
(D) Noise margin x power dissipation

h. When a flip flop is reset, its output will be

(A) $Q=0,\overline{Q}=1$ **(B)** $Q=1,\overline{Q}=0$
(C) $Q=0,\overline{Q}=0$ **(D)** $Q=1,\overline{Q}=1$

i. In a T FLIP FLOP the output frequency is

(A) Same as the input frequency **(B)** One-half of its inputs frequency
(C) Double the input frequency **(D)** None of the above

j. D flip flop can be used as a

(A) Differentiator **(B)** Divider circuit
(C) Delay Switch **(D)** None of the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a.

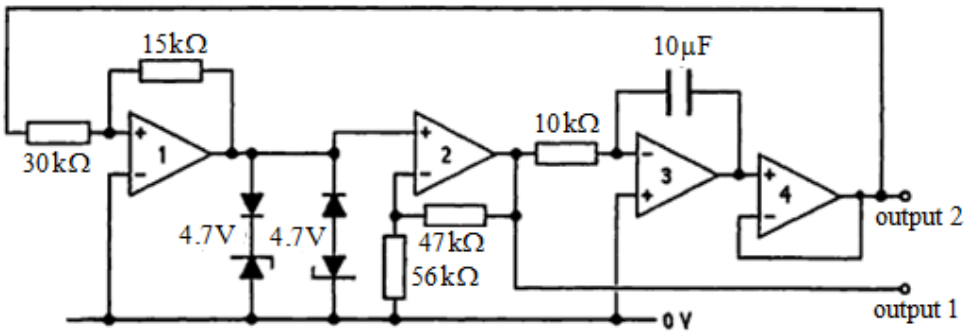

Fig.1

(i) What are the waveforms at the two outputs of the circuits of Fig.1?
(ii) What is the peak to peak amplitude of output1?
(iii) What is the peak to peak amplitude of output2?
(iv) What is the frequency of each output waveform? **(8)**

b. Determine the input and output impedances of the amplifier in the Fig.2. The op-amp data sheet gives Z_{in}=2M Ω , Z_{out} = 75 Ω , and A_{oi} =200,000. Also find the closed loop gain. **(8)**

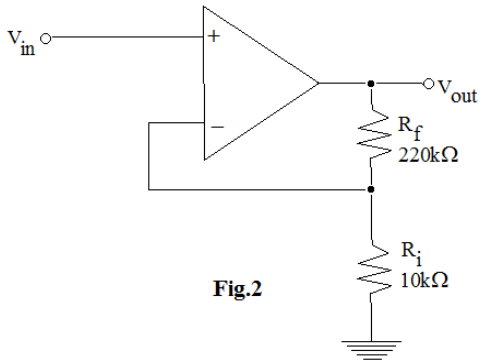

Fig.2

Q.3 a. Name the basic parts of an active filters. Explain how Butterworth, Chebyshev and Bessel responses differ. **(8)**

b. Determine the critical frequency of the low pass filter in the Fig.3, and set the value of R_1 for an approximate Butterworth response. **(8)**

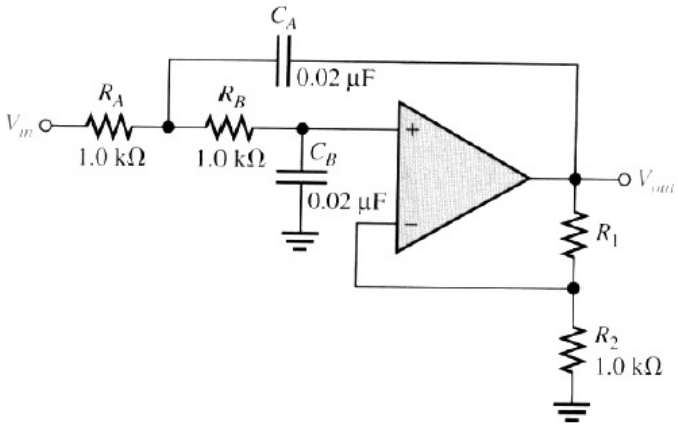

Fig.3

Q.4 a. Draw Log and antilog amplifier with a BJT. Explain the purpose of transistor perform in the log and antilog amplifier circuits. **(8)**

b. Describe the operation of digital to analog R/2R ladder DAC. Discuss resolution, accuracy, linearity, monotonicity and settling time. **(8)**

Q.5 a. (i) For the transistor switching circuit in Fig.4, what is V_{CE} When V_{IN} =0V.

(ii) What minimum value of I_B is required to saturate this Transistor if β_{DC} is 200? Assume $V_{CE\,(sat)}$ =0V.

(iii) Calculate the maximum value of R_B when V_{IN}= 5V. **(8)**

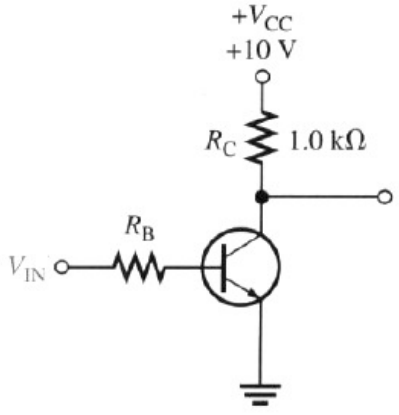

Fig.4

b. Why switching speed of a BJT is limited. How a schottky transistor can improve it? **(8)**

Q.6 a. Realize the following boolean expression using 4:1 MUX(S) only.
$Z = A'B'C'D' + A'BCD' + AB'CD' + AB'C'D + AB'C'D' + ABCD$ **(8)**

b. Implement a full adder with a decoder and two OR gates. **(8)**

Q.7 a. Design a combinational circuit using a ROM that accepts a 2-bit number and generates an output binary number equal to the square of the input number **(6)**

b. Compare TTL and ECL logic family and explain how TTL is interface to ECL. **(10)**

Q.8 a. Draw and explain the operation of four bit universal shift register. **(8)**

b. Draw and explain the operation of four bit Johnson counter. **(8)**

Q.9 a. A simple function of three inputs is given by the following expression:
$F(H) = (\overline{A}B + C)H$
(i) Construct the logic circuit by using AND/NOR/INV logic. Assume that the inputs arrive active high.
(ii) Construct the CMOS circuit for the function given in part (i).
(iii) Obtain the physical truth table for the circuit of part (ii).
(iv) Obtain the positive logic truth table for the circuit of part (ii). **(8)**

b. A system needs a 4K × 8 memory system. But the requirement is such that a single 2K × 8 RAM IC be used and the two consecutive 2K memory addresses should be overlapped to this device only? **(8)**